2018 Q4 Quarterly Reliability Report

Table of Contents

1. Introduction

Cypress's Reliability Monitor Program (RMP) is used to measure the reliability of all process technologies on a regular basis. This is an extensive effort that is aimed at providing generic fab process coverage for all fab process technologies.

The Reliability Monitor Program has two purposes:

1. Improved Reliability Performance

   Each reject is analyzed to its root cause in order to drive continuous improvement through the implementation of corrective actions.

2. Generation of Reliability Data

   RMP test results are used to assess the benefits of burn-in, provide estimates of typical lifetimes, model field applications, and determine suitability of plastic packaging in various temperature and humidity environments.

A number of process technology groupings are established for the purpose of reliability assessment. These groupings result in larger sample sizes so that the reliability analysis is statistically significant. Process similarity guidelines are used to define these process groupings.

Cypress Semiconductor has established aggressive reliability objectives. The quality standard at Cypress is zero defects, driven by a culture requiring continuous improvement in quality and reliability.

Product reliability is assured by a total quality management system. The quality management system is described in detail in Cypress Semiconductor Quality Manual. Key reliability related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing processes; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking.

Product Reliability data is accumulated as a result of new product qualification test plan activities as well as from the reliability monitor program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Sampling of device is not limited to in-house Cypress facilities but also includes certified external subcontractor foundries.

Reliability strategy requires that every failure that occurs during reliability testing be subjected to failure analysis to determine the failure mechanism. Corrective action is then implemented to prevent future failures, resulting in continuous improvement in product reliability.

Sabbas Daniel

Executive Vice-President, Quality

2. Reliability Tests and Test Conditions

The results of the RMP testing for the past six quarters are summarized in this document. The stress tests employed and the typical test conditions used are shown in the Table 2.1.

Table 2.1 Reliability Monitor Stress Conditions

Stress	Ambient Condition	Typical Read Point
Early Life	150°C, 125°C	48, 96 hours
Inherent Life	150°C, 125°C	408, 500, 1000 hours
Data Retention	150°C, 125°C	1000 hours
HAST	110°C, 85% RH	264 hours
	130°C, 85% RH	96 hours
Temperature Cycle	-40°C to 150°C (Condition M)	1000 cycles
	-55°C to 125°C (Condition B)	1000 cycles
	-65°C to 150°C (Condition C)	500 cycles
Unbiased HAST	110°C, 85% RH, no bias	264 hours
	130°C, 85% RH, no bias	96 hours
Pressure Cooker Test	121°C, 15 PSIG, no bias	96, 168 hours
High Temperature Storage	150°C, 125°C	1000 hours

Package level reliability testing refers to the assessment of the overall reliability of the device in packaged form. This consists of subjecting packaged samples to reliability tests that exposed the sample sets to different stress conditions, after which the samples are tested for any degradation.

At Cypress, plastic surface mount devices are pre-conditioned prior to undergoing Temperature Cycling, Pressure Cooker Test/Unbiased HAST, and HAST. Pre-conditioning per JEDEC Standard JESD22-A113 is required in order to simulate the stresses to which the packaged parts are subjected to during shipping, storage, board assembly and cleaning operations. Package reliability tests are performed as part of the qualification processes and as part of the standard reliability monitor program. The reliability test employed is chosen based on the failure mechanism, as different stress tests accelerate different failure mechanisms. These reliability tests utilize one or more of the following stress factors such as: temperature, moisture or humidity, voltage and pressure, to accelerate failure. Figure 2.1 shows Cypress package reliability stress flow. Packages are soaked and reflowed based on their shipping moisture sensitivity classification. The samples are tested (acoustic and electrical) after preconditioning, failures from which are considered as preconditioning failures and not reliability failures. Preconditioning failures should be taken seriously, since these imply that the samples are not robust enough to withstand the board mounting process.

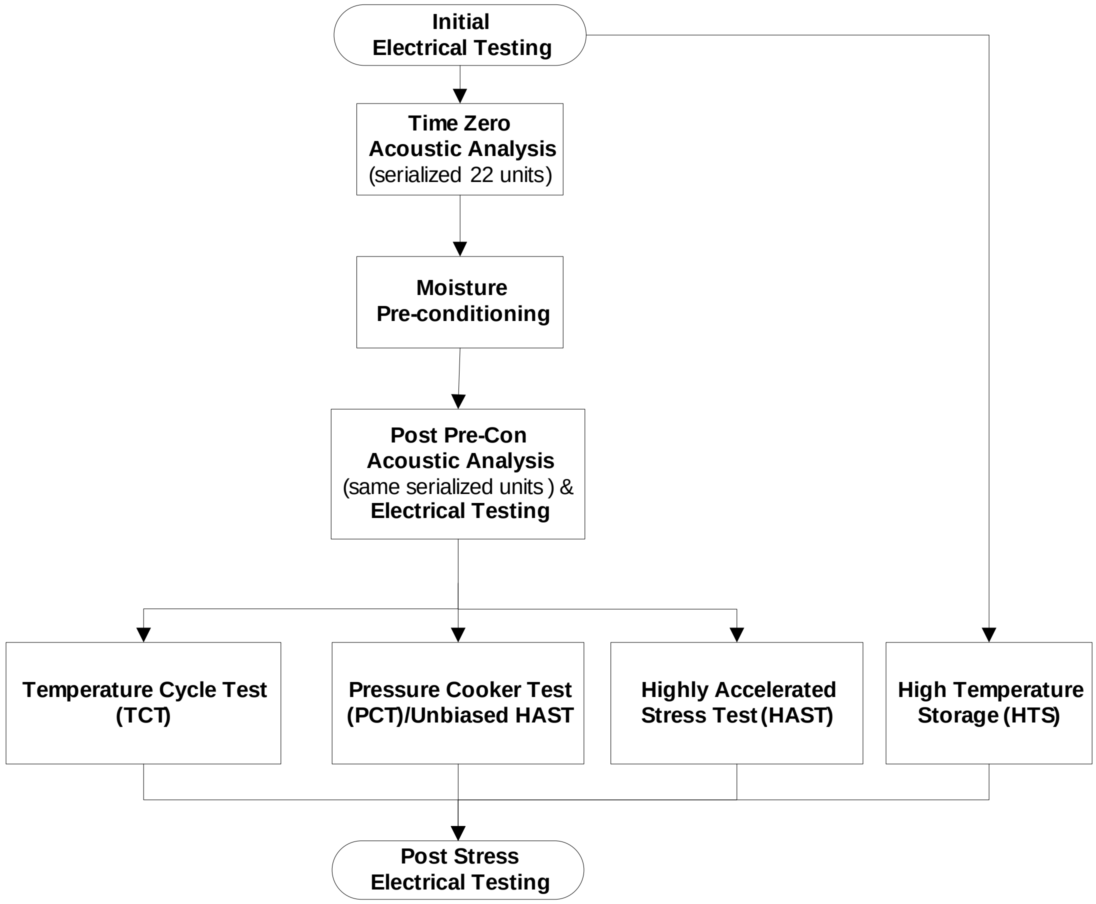


Figure 2.1 Cypress Package Reliability Stress Flow

3. Reliability Data/Analysis

The reliability data generated from the Reliability Monitor Program is presented in this section along with a detailed description of the modeling procedure used for estimating reliability under field conditions.
Also included is a summary of environmental stress results for each process technology grouping by package types.

3.1 The Exponential Distribution

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. No actual distribution can be implied as there is seldom enough data to determine one. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant.

The exponential distribution is the only one for which a MTTF (mean time to failure) value may easily be estimated and it is simply the reciprocal of the failure rate (λ). In addition, it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The conventional expression for the failure rate, λ, is

$$\lambda = \chi^2(2n + 2, 1 - \alpha)*10^9/(2*SS*t*AF)$$

where λ is the failure rate in FITs (failures per billion unit-hours), $\chi^2(2n+2,1-\alpha)/2$ is the upper confidence value for "**n**" failures and upper confidence limit, (expressed as a decimal value), **SS** is the sample size, t is the test duration in hours, and **AF** is the acceleration factor relating the life test junction temperature to a assumed field junction temperature.

The χ^2(chi square) value for 2n+2 degrees of freedom and the probability, 1-α, can be obtained from a table or calculated using Microsoft® Excel chi squared inverse function [=CHIINV(1-α,2n+2)].

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-part sample from a certain product population had one failure and a 60% confidence level was desired. The chi square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the "true" value of the population's defect rate is between zero (or some very small value) and 2.02%.

3.2 Failure Distributions

The lognormal and Weibull CDF's are the distributions most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The lognormal distribution is specified by two parameters: T_{50}, the median time to failure, and sigma, the shape parameter. Similarly, the Weibull distribution, which can be written in closed form as

$$F(t) = 1 - \exp[-(t/c)^m],$$

is characterized by a characteristic life c and a shape parameter m. The value of the shape parameter determines whether the failure rate is increasing (m>1), decreasing (m<1), or constant (m=1). The exponential distribution, is specified completely by the one parameter c which is called the mean time to failure (MTTF). Figures 1 and 2 show failure rates for several values of the scale parameters of the lognormal and Weibull distributions, respectively.

$$F(t) = 1 - \exp[-(t/c)],$$

Figure 1. Lognormal Distribution

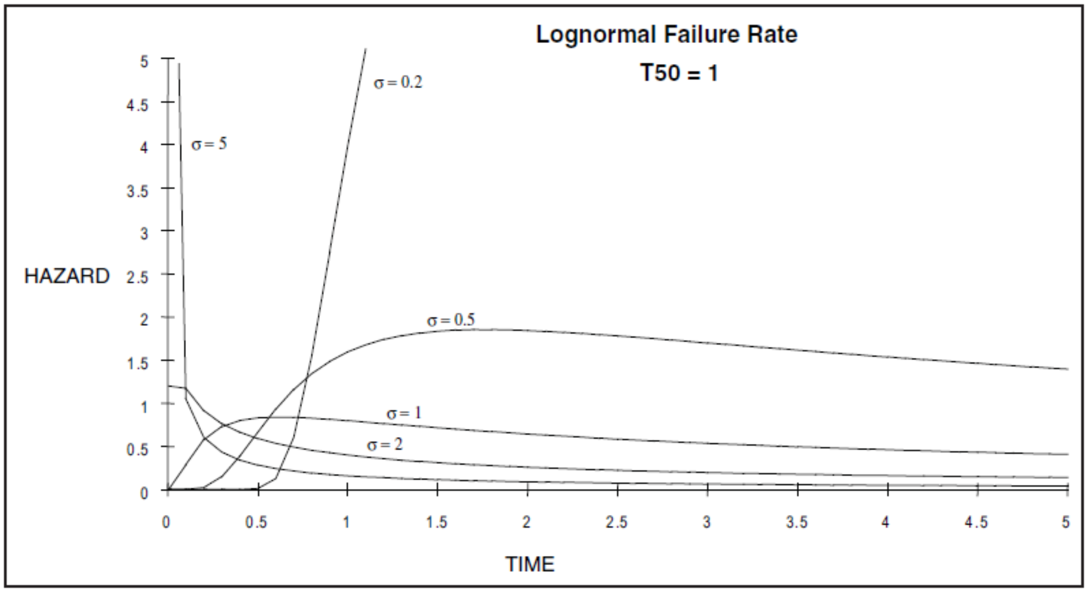
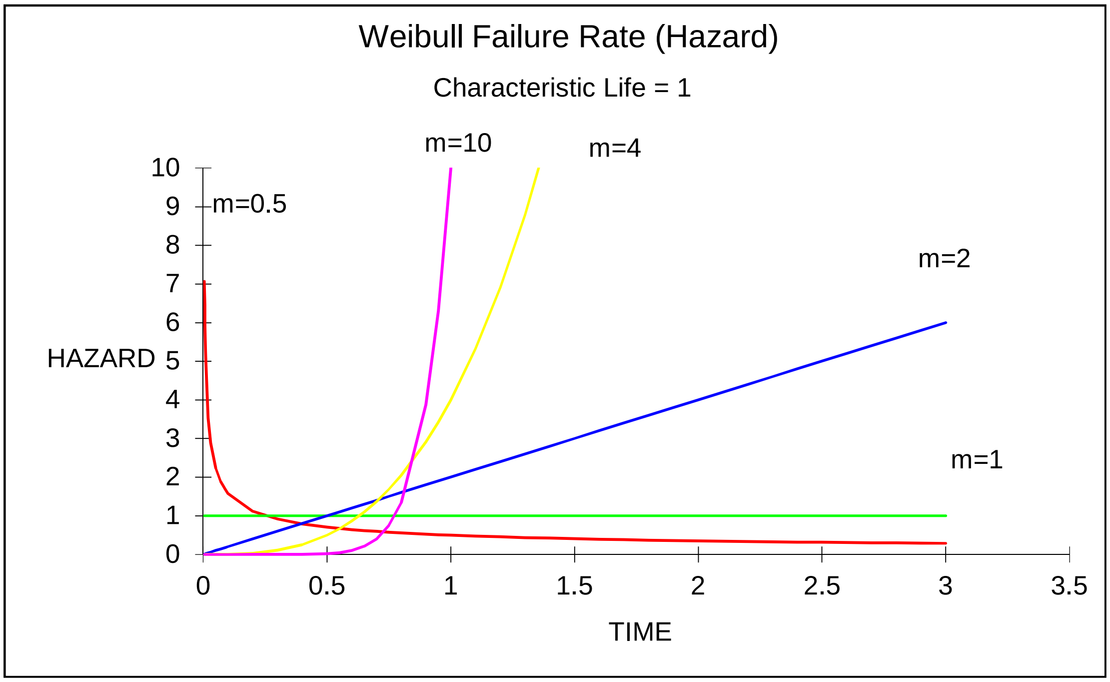


Figure 2. Weibull Distribution



3.3 Calculations of Failure Rates

To estimate field failure rates from reliability studies, many factors must be considered. One primary requirement is the identification of individual failure mechanisms in order to ascribe the failures to the proper categories used in the Cypress reliability model.

3.3.1 Considerations and Assumptions

1. Defective subpopulations and Early Life failures:

   In any production lot, a defective subpopulation may exist. These are devices that fail by a mechanism that is not common to the general population and is usually the result of some processing error or defect. These failures usually occur early and consequently called Early Life failures. Early life reliability is reported in terms of ppm defective expected during the first year of use under typical use conditions. No upper confidence bound will be used for this estimate. The ppm defective is the ration of the number of rejects to the number of samples and expressed in ppm.

   PPM = (Total Reject / Total samples) * 1,000,000

2. Inherent Life failures:

   Failures that occur in later life reliability are usually caused by mechanisms related to defects that could occur in any product of this type. These are known here as Inherent Life failures. Inherent life reliability is reported in using the exponential model, in terms of FITs (failures per billion unit-hours) with a 60% upper confidence bound for zero failure.

3. Estimation of thermal acceleration factors:

   The best-known activation energies for each mechanism are used in calculating the thermal acceleration using the standard Arrhenius equation for thermal acceleration. For each process group/ package combination, representative acceleration factors were estimated based on the weighted average of acceleration factors of individual devices in that group.

4. Voltage acceleration factor is not included in failure rate calculation even though voltage acceleration may be used during stress.

5. It is common in reliability literature to see failure rates stated at a specified level of confidence:

   For example, a 60% upper confidence limit on the failure rate indicates that unless a 4 in 10 chances (40%) has occurred, the true population failure rate is less than the stated limit. The summation of individual failure rate components, each at 60% confidence, will however, result in an overall failure rate at an unknown confidence level that may dramatically exceed 60%. The failure rates quoted in the Quarterly Reliability Report are at a 60% upper confidence level.

4. Data Summaries by Process Technology

Technology	Products Family	Inherent Life (FITS)
CS 69S, CS 69LS	S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families	5
CS 69SS, CS 69LSS	S29AL-J, S29AS-J, S29JL-J Product Families	4
CS 119S, CS 119LS	S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL- N, S71WS-N Product Families	5
CS 129, CS 129L, CS 129AL	S19FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families	4
CS239, CS239L, CS 239LS	S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S, S29VS-R, S29WS-R Product Families	11
CS 340L	S29GL-T Product Families	16
90 nm SPI Floating Gate	S25FL1-K, S25FL2-K Product Families	3
65nm SPI Floating Gate	S25FL-L Product Families	6
48 nm SLC NAND	S34ML-1 Product Families	14
41 nm SLC NAND	S34ML-1 Product Families	9
32 nm SLC NAND	S34ML-2 Product Families	9
C8	HSLS_USB (CY7C64713*, CY7C68013A*) Product Families	24
C9	ASYNC (CY62128ELL*, CY62138FV30LL*,CY62167/77EV30LL*, CY7C1021D*) Product Families	25
LL65	SYNC (CY7C1361KE33*), ASYNC (CY62167EV30LL*,CY62167G30*, CY7C1061G30*) Product Families	11
P26	HSLS_USB (CY7C63743CK4*) Product Families	**
R42	SPCM (CY7C144E*), ASYNC (CY62167DV30LL*) Product Families	**
R52	ASYNC (CY621282BNLL*) Product Families	**
R7	ASYNC (CY7C1041CV33*) Product Families	**
R8	ASYNC (CY62167DV30*) Product Families	**
R9	SYNC (CY7C1480BV33*, CY7C1471BV33*, CY7C1472BV33*) Product Families	24
R95	ASYNC (CY62128ELL*, CY62126EV30LL*, CY62146ESL*, CY62147EV30LL*, CY62167EV18LL *, CY62177EV30LL*) Product Families	9
S4	AUTOPSOC (CY8C21645*, CY8C29666*, CY8C21534*) Product Families	**
S40	PSOC (CY7CS40T3A*) Product Families	**
S8	NVSRAM (CY14B101*, CY14B104*, CY14B116N*, CY14V101*, CY14V104*); CLOCKS (CY27430FL*); AUTOPSOC (CY8C4024*, CY8C4025*, CY8C4045*, CY8CTMA616*, CYAT81688*, CYAT817AZS72*); PSOC (CY8C4014*, CY8C4124*, CY8C4127*, CY8C4146*, CY8C4147*, CY8C4245*,CY8C5667*, CY8C5668*, CY8C6247*, CY8C6347*, CY8CMBR3108*); WUSB (CYBL10161*, CYBL10162*, CYBL10462*, CYBL10561*, CYBL10563*, CYBL111712*); TYPE-C (CYPDC1185*, CYPD2122*, CYPD2703*, CYPD3135*, CYPD3171*, CYPD3175*, CYPD41257*, CYPD4226*, CYPD5126*, CYPD5225*); TT (CYTMA445A*, CYTMA450E*) Product Families	1
130nm TI F-RAM	F-RAM (CY15B102N*, CY15B104Q7*, FM22L167*, FM25V01*) Product Families	9
180nm PMICs	S6AXXXX, S6BXXXX Product Families	24
40 nm MCU (FLASH)	S6J33X, S6J34X, S6J35X Product Families	27
55nm MCU (FLASH)	S6J31X, S6J32X Product Families	23
90nm MCU (FLASH)	S6E1XXX, S6E2XXX, CY(MB)9AFXXX, CY(MB)9BFXXX, CY(MB)9DFXXX, CY(MB)9EFXXX, CY(MB)91F52X Product Families	**
180nm MCU (FLASH)	CY(MB)90FXXX, CY(MB)91FXXX, CY(MB)95F5XX, CY(MB)95F6XX Product Families	6
350 nm MCU (FLASH)	CY(MB)90F3XX, CY(MB)91F3XX, CY(MB)95F1XX Product Families	**

Note:
***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.1 S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families

CS 69S, CS 69LS

This 0.11 micron CMOS Flash technology was introduced in December 2003 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	1000							
Sample Size	2950	840							
150C, Zero fails, Process ave. Ea	0	0	0.7	217	1	217	22739	0	5

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	922	0	0	<1

4.2 S29AL-J, S29AS-J, S29JL-J Product Families

CS 69SS, CS 69LSS

This 0.11 micron CMOS Flash technology was introduced in February 2008 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	1000							
Sample Size	4100	1074							
150C, Zero fails, Process ave. Ea	0	0	0.7	227	1	227	30414	0	4

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	924	0	0	<1

4.3 S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL-N, S71WS-N Product Families

CS 119S, CS 119LS

This 0.11 micron CMOS Flash technology was introduced in June 2004 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three or four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	1000							
Sample Size	3700	900							
150C, Zero fails, Process ave. Ea	0	0	0.7	196	1	196	21994	0	5

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	462	0	0	<1

4.4 S19FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families

CS 129, CS 129L, CS 129AL

This 90 nanometer CMOS Flash technology was introduced in Aug 2006 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three copper layers.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	1000							
Sample Size	3300	1140							
150C, Zero fails, Process ave. Ea	0	0	0.7	188	1	188	26632	0	4

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	924	0	0	<1

4.5 S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S, S29VS-R, S29WS-R Product Families

CS 239, CS 239L, CS 239LS

This 65 nm Mirror bit flash technology was introduced in September 2010 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	1000							
Sample Size	800	2350	1180							
125C, Zero fails, Process ave. Ea	0	0	0	0.7	69	1	69	10123	0	11

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	2120	0	0	<1

4.6 S29GL-T Product Families

CS 340L

This 45nm Mirror bit flash technology was introduced in December 2015 and utilizes a tunnel oxide, Silicon Nitride(SiN) data storage layer, silicided poly word and interconnections are four metal layers with contact plu and five metal layers with contact plug and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	1000							
Sample Size	1558	2000	1404							
125C, Zero fails, Process ave. Ea	0	0	0	0.7	40	1	40	6960	0	16

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	462	0	0	<1

4.7 S25FL1-K, S25FL2-K Product Families

90 nm SPI Floating Gate

90 nm SPI (Serial Peripheral Interface) Floating Gate Flash Technology was introduced in May 2012 and utilizes tunnel oxide, polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	1000							
Sample Size	3450	1276							
150C, Zero fails, Process ave. Ea	0	0	0.7	208	1	208	33142	0	3

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	462	0	0	<1

4.8 S25FL-L Product Families

65 nm SPI Floating Gate

65nm SPI (Serial Peripheral Interface) Floating Gate Technology was introduced in August 2016 and utilizes tunnel oxide, polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	1000							
Sample Size	2150	700							
150C, Zero fails, Process ave. Ea	0	0	0.7	227	1	227	19823	0	6

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	385	0	0	<1

4.9 S34ML-1 Product Families

48 nm SLC NAND

48 nm SLC NAND was introduced in July 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 48 nm SLC NAND is using Tungsten.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	1000							
Sample Size	1600	2500	900							
125C, Zero fails, Process ave. Ea	0	0	0	0.7	74	1	74	8317	0	14

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	539	0	0	<1

4.10 S34ML-1 Product Families

41 nm SLC NAND

41 nm SLC NAND were introduced in Jun 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 41 nm SLC NAND is using Copper.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	1000							
Sample Size	800	2500	1346							
125C, Zero fails, Process ave. Ea	0	0	0	0.7	74	1	74	12438	0	9

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	847	0	0	<1

4.11 S34ML-2 Product Families

32 nm SLC NAND

32 nm SLC NAND were introduced in October 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 32 nm SLC NAND is using Copper

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	1000							
Sample Size	1080	2500	1440							
125C, Zero fails, Process ave. Ea	0	0	0	0.7	74	1	74	13307	0	9

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	924	0	0	<1

4.12 HSLS_USB (CY7C64713*, CY7C68013A*) Product Families

C8 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	**1000**							
Sample Size	705	705							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	4857	0	24

4.13 ASYNC (CY62128ELL*, CY62138FV30LL*,CY62167/77EV30LL*, CY7C1021D*) Product Families

C9 Technology

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		77			77						0	25
125C, Zero fails, Process ave. Ea		0			0	0.7	55	1	55			
Sample Size	3097		240	193								
150C, Zero fails, Process ave. Ea	0		0	0		0.7	170	1	170	4645		

4.14 SYNC (CY7C1361KE33*), ASYNC (CY62167EV30LL*,CY62167G30*, CY7C1061G30*) Product Families

LL65 Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500	1000							
Sample Size		5789		729						0	11
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	5055		480								
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170	10102		

4.15 HSLS_USB (CY7C63743CK4*) Product Families

P26 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	3040	232							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	2455	0	**

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	160	0	0	34

4.16 SPCM (CY7C144E*), ASYNC (CY62167DV30LL*) Product Families

R42 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	392	392							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	2701	0	**

4.17 ASYNC (CY621282BNLL*) Product Families

R52 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	**408**							
Sample Size	1598	160							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	1382	0	**

4.18 ASYNC (CY7C1041CV33*) Product Families

R7 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	**408**							
Sample Size	77	77							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	665	0	**

4.19 ASYNC (CY62167DV30*) Product Families

R8 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	154	154							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	1630	0	**

4.20 SYNC (CY7C1480BV33*, CY7C1471BV33*, CY7C1472BV33*) Product Families

R9 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	455	455							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	4815	0	24

4.21 ASYNC (CY62128ELL*, CY62126EV30LL*, CY62146ESL*, CY62147EV30LL*, CY62167EV18LL *, CY62177EV30LL*) Product Families

R95 Technology

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		6982			351						0	9
125C, Zero fails, Process ave. Ea		0			0	0.7	55	1	55			
Sample Size	1145		798	347								
150C, Zero fails, Process ave. Ea	0		0	0		0.7	170	1	170	12981		

4.22 AUTOPSOC (CY8C21645*, CY8C29666*, CY8C21534*) Product Families

S4 Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	1000							
Sample Size		2376		240							
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	80		80							0	**
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			
									2344		

4.23 PSOC (CY7CS40T3A*) Product Families

S40 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	396	396							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	2728	0	**

4.24 NVSRAM (CY14B101*, CY14B104*, CY14B116N*, CY14V101*, CY14V104*); CLOCKS (CY27430FL*); AUTOPSOC (CY8C4024*, CY8C4025*, CY8C4045*, CY8CTMA616*, CYAT81688*, CYAT817AZS72*); PSOC (CY8C4014*, CY8C4124*,CY8C4127*, CY8C4146*, CY8C4147*, CY8C4245*,CY8C5667*, CY8C5668*, CY8C6247*, CY8C6347*, CY8CMBR3108*); WUSB (CYBL10161*, CYBL10162*, CYBL10462*, CYBL10561*, CYBL10563*, CYBL111712*); TYPE-C (CYPDC1185*, CYPD2122*, CYPD2703*, CYPD3135*, CYPD3171*, CYPD3175*, CYPD41257*, CYPD4226*, CYPD5126*, CYPD5225*); TT (CYTMA445A*, CYTMA450E*) Product Families

S8 Technology

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		2328			683							
125C, Zero fails, Process ave. Ea		0			0	0.7	55	1	55			
Sample Size	95548		1309	6525							0	1
150C, Zero fails, Process ave. Ea	0		0	0		0.7	170	1	170	85055		

Data Retention Bake – 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	1040	0	0	5

4.25 F-RAM (CY15B102N*, CY15B104Q7*, FM22L167*, FM25V01*) Product Families

130nm TI F-RAM Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	10696	1872							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	12897	0	9

Data Retention Bake – 125/150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000 (125)	1171	0	0	<1
1000 (150)	158	0	0	

4.26 S6AXXXX, S6BXXXX Product Families

180 nm PMICs

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	693	693							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	4774	0	24

4.27 S6J33X, S6J34X, S6J35X Product Families

40 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	**1000**							
Sample Size	616	616							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	4244	0	27

4.28 S6J31X, S6J32X Product Families

55 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	252	252							
105C, Zero fails, Process ave. Ea	0	0	0.7	20	1	20			
Sample Size	616	616						0	23
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55			
							4882		

4.29 S6E1XXX, S6E2XXX, CY(MB)9AFXXX, CY(MB)9BFXXX, CY(MB)9DFXXX, CY(MB)9EFXXX, CY(MB)91F52X Product Families

90 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	356	356							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	2453	0	**

4.30 CY(MB)90FXXX, CY(MB)91FXXX, CY(MB)95F5XX, CY(MB)95F6XX Product Families

180 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	2990	2990							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	20600	0	6

4.31 CY(MB)90F3XX, CY(MB)91F3XX, CY(MB)95F1XX Product Families

350 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	348	348							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	2398	0	**

5. Data Summaries by Package Family

5.1 BGA (Ball Grid Array)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	667	0	0
	264hrs	1785	0	0
HIGH TEMP STORAGE	1000hrs	4104	0	0
PRESSURE COOKER TEST	168hrs	80	0	0
TEMP CYCLE	500cycle	2493	0	0
	1000cycle	2364	0	0
UNBIASED HAST TEST	96hrs	3634	0	0
	264hrs	250	0	0

5.2 BGA (Ball Grid Array) – Flip Chip

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HIGH TEMP STORAGE	1000hrs	325	0	0
TEMP CYCLE	1000cycle	305	0	0
UNBIASED HAST TEST	96hrs	325	0	0

5.3 DFN (Dual Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	379	0	0
HIGH TEMP STORAGE	1000hrs	773	0	0
PRESSURE COOKER TEST	168hrs	465	0	0
TEMP CYCLE	500cycle	503	0	0
	1000cycle	125	0	0
UNBIASED HAST TEST	96hrs	125	0	0

5.4 DIP (Dual-In-line Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	90	0	0
HIGH TEMP STORAGE	1000hrs	330	0	0
PRESSURE COOKER TEST	168hrs	208	0	0
TEMP CYCLE	500cycle	358	0	0
UNBIASED HAST TEST	96hrs	150	0	0

5.5 QFN (Quad Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	2951	0	0
HIGH TEMP STORAGE	1000hrs	2916	0	0
PRESSURE COOKER TEST	96hrs	1160	0	0
	168hrs	4143	0	0
TEMP CYCLE	500cycle	6611	0	0
	1000cycle	225	0	0
UNBIASED HAST TEST	96hrs	1939	0	0

5.6 QFP (Quad Flat Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	6762	0	0
	264hrs	375	0	0
HIGH TEMP STORAGE	1000hrs	5602	0	0
PRESSURE COOKER TEST	96hrs	1869	0	0
	168hrs	1613	0	0
TEMP CYCLE	500cycle	13871	0	0
	1000cycle	385	0	0
UNBIASED HAST TEST	96hrs	8723	0	0

5.7 SOJ (Small Outline J Lead)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	289	0	0
HIGH TEMP STORAGE	1000hrs	270	0	0
PRESSURE COOKER TEST	168hrs	214	0	0
TEMP CYCLE	500cycle	734	0	0
UNBIASED HAST TEST	96hrs	308	0	0

5.8 SOP (Small Outline Gull Wing Lead Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	3126	0	0
HIGH TEMP STORAGE	1000hrs	3408	0	0
PRESSURE COOKER TEST	96hrs	388	0	0
	168hrs	2299	0	0
TEMP CYCLE	500cycle	3773	0	0
	1000cycle	1273	0	0
UNBIASED HAST TEST	96hrs	1388	0	0

5.9 SSOP (Shrink Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1894	0	0
HIGH TEMP STORAGE	1000hrs	986	0	0
PRESSURE COOKER TEST	96hrs	1117	0	0
	168hrs	1195	0	0
TEMP CYCLE	500cycle	2412	0	0
UNBIASED HAST TEST	96hrs	154	0	0

5.10 TSOP (Thin Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	4969	0	0
	264hrs	438	0	0
HIGH TEMP STORAGE	1000hrs	5650	0	0
PRESSURE COOKER TEST	96hrs	640	0	0
	168hrs	2532	0	0
TEMP CYCLE	500cycle	5182	0	0
	1000cycle	1592	0	0
UNBIASED HAST TEST	96hrs	3438	0	0

5.11 WLCSP (Wafer Level Chip Scale Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	298	0	0
	264hrs	30	0	0
HIGH TEMP STORAGE	1000hrs	772	0	0
PRESSURE COOKER TEST	96hrs	160	0	0
TEMP CYCLE	1000cycle	2308	0	0
UNBIASED HAST TEST	96hrs	3098	0	0
	264hrs	77	0	0

Document History Page

Document Title: 2018 Q4 QUARTERLY RELIABILITY REPORT
Document Number: 002-26089

Rev.	ECN No.	Orig. of Change	Description of Change
**	6423888	BHGO	Initial Spec Release