2017 Q4 Quarterly Reliability Report

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1. Introduction

Cypress's Reliability Monitor Program (RMP) is used to measure the reliability of all process technologies on a regular basis. This is an extensive effort that is aimed at providing generic fab process coverage for all fab process technologies.

The Reliability Monitor Program has two purposes:

1. Improved Reliability Performance

   Each reject is analyzed to its root cause in order to drive continuous improvement through the implementation of corrective actions.

2. Generation of Reliability Data

   RMP test results are used to assess the benefits of burn-in, provide estimates of typical lifetimes, model field applications, and determine suitability of plastic packaging in various temperature and humidity environments.

A number of process technology groupings are established for the purpose of reliability assessment. These groupings result in larger sample sizes so that the reliability analysis is statistically significant. Process similarity guidelines are used to define these process groupings.

Cypress Semiconductor has established aggressive reliability objectives. The quality standard at Cypress is zero defects, driven by a culture requiring continuous improvement in quality and reliability.

Product reliability is assured by a total quality management system. The quality management system is described in detail in Cypress Semiconductor Quality Manual. Key reliability related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing processes; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking.

Product Reliability data is accumulated as a result of new product qualification test plan activities as well as from the reliability monitor program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Sampling of device is not limited to in-house Cypress facilities but also includes certified external subcontractor foundries.

Reliability strategy requires that every failure that occurs during reliability testing be subjected to failure analysis to determine the failure mechanism. Corrective action is then implemented to prevent future failures, resulting in continuous improvement in product reliability.

Sabbas Daniel

Executive Vice-President, Quality

2. Reliability Tests and Test Conditions

The results of the RMP testing for the past six quarters are summarized in this document. The stress tests employed and the typical test conditions used are shown in the Table 2.1.

Table 2.1 Reliability Monitor Stress Conditions

Stress	Ambient Condition	Typical Read Point
Early Life	150°C, 125°C	48, 96 hours
Inherent Life	150°C, 125°C	168, 408, 500, 1000 hours
Data Retention	150°C, 125°C	1000 hours
HAST	110°C, 85% RH 130°C, 85% RH	264 hours 96 hours
Temperature Cycle	-40°C to 150°C (Condition M) -55°C to 125°C (Condition B) -65°C to 150°C (Condition C)	1000 cycles 1000 cycles 500 cycles
Unbiased HAST	110°C, 85% RH, no bias 130°C, 85% RH, no bias	264 hours 96 hours
Pressure Cooker Test	121°C, 15 PSIG, no bias	96, 168 hours
High Temperature Storage	150°C, 125°C	1000 hours

Package level reliability testing refers to the assessment of the overall reliability of the device in packaged form. This consists of subjecting packaged samples to reliability tests that exposed the sample sets to different stress conditions, after which the samples are tested for any degradation.

At Cypress, plastic surface mount devices are pre-conditioned prior to undergoing Temperature Cycling, Pressure Cooker Test/Unbiased HAST, and HAST. Pre-conditioning per JEDEC Standard JESD22-A113 is required in order to simulate the stresses to which the packaged parts are subjected to during shipping, storage, board assembly and cleaning operations. Package reliability tests are performed as part of the qualification processes and as part of the standard reliability monitor program. The reliability test employed is chosen based on the failure mechanism, as different stress tests accelerate different failure mechanisms. These reliability tests utilize one or more of the following stress factors such as: temperature, moisture or humidity, voltage and pressure, to accelerate failure. Figure 2.1 shows Cypress package reliability stress flow. Packages are soaked and reflowed based on their shipping moisture sensitivity classification. The samples are tested (acoustic and electrical) after preconditioning, failures from which are considered as preconditioning failures and not reliability failures. Preconditioning failures should be taken seriously, since these imply that the samples are not robust enough to withstand the board mounting process.

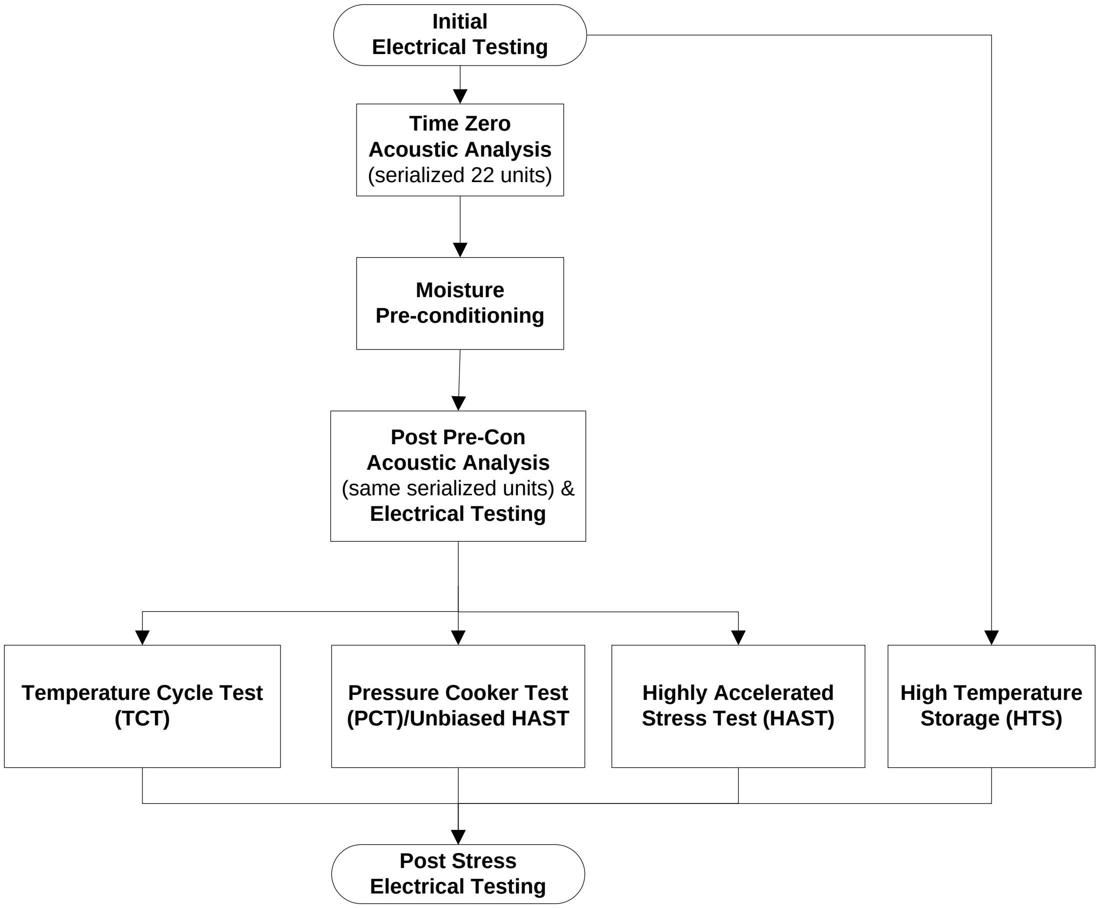


Figure 2.1 Cypress Package Reliability Stress Flow

3. Reliability Data/Analysis

The reliability data generated from the Reliability Monitor Program is presented in this section along with a detailed description of the modeling procedure used for estimating reliability under field conditions.
Also included is a summary of environmental stress results for each process technology grouping by package types.

3.1 The Exponential Distribution

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. No actual distribution can be implied as there is seldom enough data to determine one. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant.

The exponential distribution is the only one for which a MTTF (mean time to failure) value may easily be estimated and it is simply the reciprocal of the failure rate (λ). In addition, it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The conventional expression for the failure rate, λ, is

$$\lambda = \chi^2(2n + 2, 1 - \alpha)*10^9/(2*SS*t*AF)$$

where λ is the failure rate in FITs (failures per billion unit-hours), $\chi^2(2n+2,1-\alpha)/2$ is the upper confidence value for "**n**" failures and upper confidence limit, (expressed as a decimal value), **SS** is the sample size, t is the test duration in hours, and **AF** is the acceleration factor relating the life test junction temperature to a assumed field junction temperature.

The χ^2(chi square) value for 2n+2 degrees of freedom and the probability, 1-α, can be obtained from a table or calculated using Microsoft® Excel chi squared inverse function [=CHIINV(1-α,2n+2)].

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-part sample from a certain product population had one failure and a 60% confidence level was desired. The chi square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the "true" value of the population's defect rate is between zero (or some very small value) and 2.02%.

3.2 Failure Distributions

The lognormal and Weibull CDF's are the distributions most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The lognormal distribution is specified by two parameters: T_{50}, the median time to failure, and sigma, the shape parameter. Similarly, the Weibull distribution, which can be written in closed form as

$$F(t) = 1 - \exp[-(t/c)^m],$$

is characterized by a characteristic life c and a shape parameter m. The value of the shape parameter determines whether the failure rate is increasing (m>1), decreasing (m<1), or constant (m=1). The exponential distribution, is specified completely by the one parameter c which is called the mean time to failure (MTTF). Figures 1 and 2 show failure rates for several values of the scale parameters of the lognormal and Weibull distributions, respectively.

$$F(t) = 1 - \exp[-(t/c)],$$

Figure 1. Lognormal Distribution

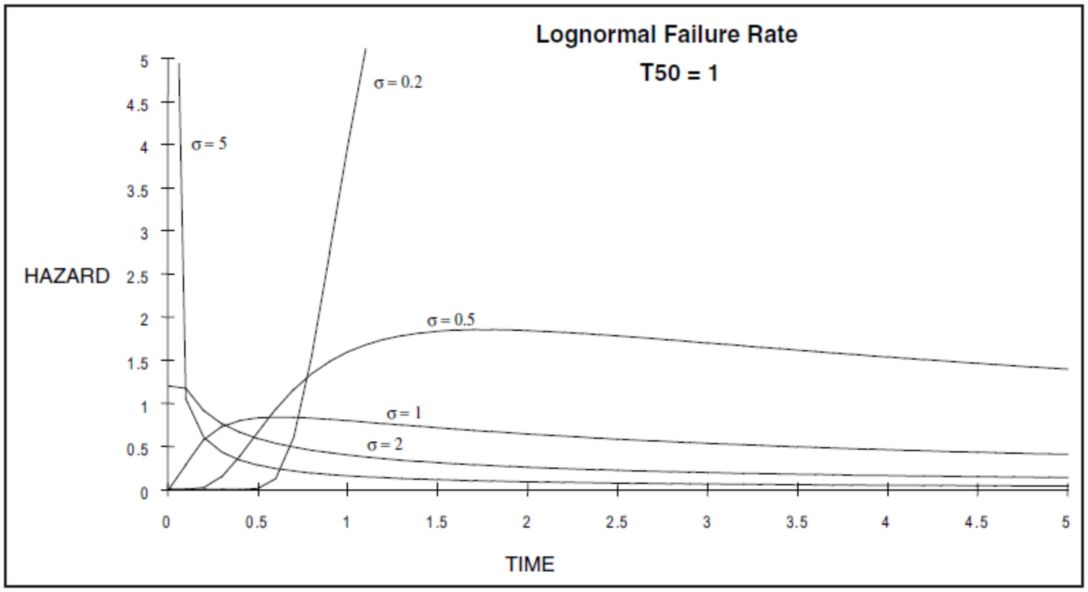
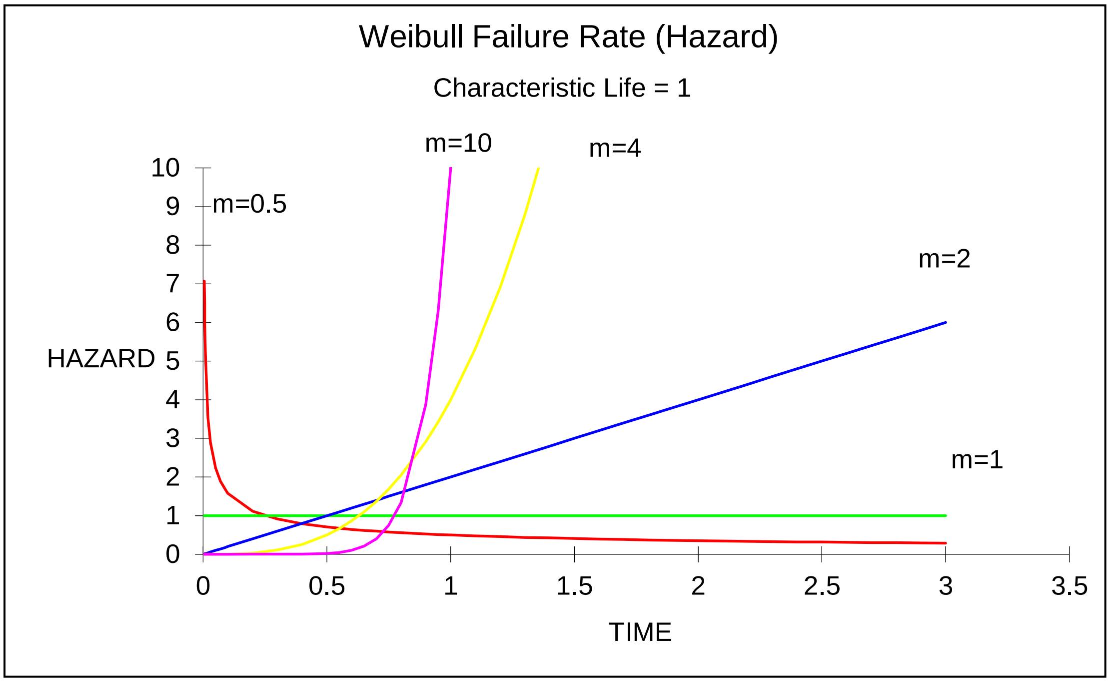


Figure 2. Weibull Distribution



3.3 Calculations of Failure Rates

To estimate field failure rates from reliability studies, many factors must be considered. One primary requirement is the identification of individual failure mechanisms in order to ascribe the failures to the proper categories used in the Cypress reliability model.

3.3.1 Considerations and Assumptions

1. Defective subpopulations and Early Life failures:

   In any production lot, a defective subpopulation may exist. These are devices that fail by a mechanism that is not common to the general population and is usually the result of some processing error or defect. These failures usually occur early and consequently called Early Life failures. Early life reliability is reported in terms of ppm defective expected during the first year of use under typical use conditions. No upper confidence bound will be used for this estimate. The ppm defective is the ration of the number of rejects to the number of samples and expressed in ppm.

   PPM = (Total Reject / Total samples) * 1,000,000

2. Inherent Life failures:

   Failures that occur in later life reliability are usually caused by mechanisms related to defects that could occur in any product of this type. These are known here as Inherent Life failures. Inherent life reliability is reported in using the exponential model, in terms of FITs (failures per billion unit-hours) with a 60% upper confidence bound for zero failure.

3. Estimation of thermal acceleration factors:

   The best-known activation energies for each mechanism are used in calculating the thermal acceleration using the standard Arrhenius equation for thermal acceleration. For each process group/ package combination, representative acceleration factors were estimated based on the weighted average of acceleration factors of individual devices in that group.

4. Voltage acceleration factor is not included in failure rate calculation even though voltage acceleration may be used during stress.

5. It is common in reliability literature to see failure rates stated at a specified level of confidence:

   For example, a 60% upper confidence limit on the failure rate indicates that unless a 4 in 10 chances (40%) has occurred, the true population failure rate is less than the stated limit. The summation of individual failure rate components, each at 60% confidence, will however, result in an overall failure rate at an unknown confidence level that may dramatically exceed 60%. The failure rates quoted in the Quarterly Reliability Report are at a 60% upper confidence level.

4. Data Summaries by Process Technology

Technology	Products Family	Inherent Life (FITS)
CS 69S, CS 69LS	S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families	3
CS 69SS, CS 69LSS	S29AL-J, S29AS-J, S29JL-J Product Families	2
CS 119S, CS 119LS	S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL- N, S71WS-N Product Families	4
CS 129, CS 129L, CS 129AL	S19FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families	3
CS 239LS	S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S Product Families	8
CS 340L	S29GL-T Product Families	26
90 nm SPI Floating Gate	S25FL1-K, S25FL2-K Product Families	3
48 nm SLC NAND	S34ML-1 Product Families	7
41 nm SLC NAND	S34ML-1 Product Families	7
32 nm SLC NAND	S34ML-2 Product Families	7
C8	HSLS_USB (CY7C64713*, CY7C68013A*) Product Families	**
C9	ASYNC (CY7C1041D*) Product Families	**
LL65	SYNC (CY7C1460K*); HRUSB (CYUSB3304*, CYUSB2302*) Product Families	17
LP55	CLOCKS (CY29430F*) Product Families	18
R7	ASYNC (CY7C1061AV*, CY7C1041CV33*) Product Families	**
R8	ASYNC (CY62167DV30*) Product Families	**
R42	SPCM (CY7C144E*)	**
R9	SYNC (CY7C1380D*, CY7C1471BV33D*) Product Families	**
R95	ASYNC (CY62147EV30LL*, CY62167EV18LL*, CY62167EV30LL*) Product Families	13
S4	AUTOPSOC (CY8C21334*, CY8C21534*, CY8C29466*, CY8CTMA120); PSOC (CY8C4124*, CY8C4125*) Product Families	20
S8	NVSRAM (CY14B101*, CY14B104*, CY14B108L*, CY14B116L*); AUTOPSOC (CY8C20236A*, CY8CTMA461* CY8CTMA616*, CYAT81688*, CY8C4245*); PSOC (CY8C3866A*, CY8C4124, CY8C4125*, CY8C4245* CY8C4146*, CY8C4246*, CY8C4248*); TYPE-C (CYPD21222*, CYPD21227*, CYPD21228*, CYPD21342*, CYPD3135*, CYPD4226*, CYPD5225); TT (TT21100*, CYTT21403*, CYTT21402*, CYAT81688*, CYTMA445A*); WUSB (CYBL10161*, CYBL10563*) Product Families	1
130nm TI F-RAM	F-RAM (CY15B064*, CY15B102N*, CY15B102Q7*, CY15B104Q7*, CY15B256*, CY15E064J*, FM24C16B7*, FM24V107*, FM24CL64B7*, FM25040B7*, FM25V20A7*, FM25V01*, FM25V107*, FM28V202*) Product Families	6
180nm PMICs	S6AXXXX, S6BXXXX Product Families	10
40 nm MCU (FLASH)	S6J33X, S6J34X Product Families	7
55nm MCU (FLASH)	S6J31X, S6J32X Product Families	22
90nm MCU (FLASH)	S6E1XXX, S6E2XXX, MB9AF11X, MB91F52X Product Families	6
180nm MCU (FLASH)	MB91F4XX, MB95F5XX, MB95F6XX Product Families	5
350 nm MCU (FLASH)	MB90F3XX, MB91F3XX, MB95F1XX Product Families	13

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.1 S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families

CS 69S, CS 69LS

This 0.11 micron CMOS Flash technology was introduced in December 2003 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	2370	3300	5170	960	60							
150C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	217	1	217	40040	0	3

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1078	0	0	<1
1000	1078	0	0	
2000	384	0	0	

4.2 S29AL-J, S29AS-J, S29JL-J Product Families

CS 69SS, CS 69LSS

This 0.11 micron CMOS Flash technology was introduced in February 2008 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	1100	4050	5000	1391	80							
150C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	227	1	227	52029	0	2

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1001	0	0	<1
1000	1078	0	0	
2000	923	0	0	

4.3 S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL-N, S71WS-N Product Families

CS 119S, CS 119LS

This 0.11 micron CMOS Flash technology was introduced in June 2004 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three or four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	1100	4300	4899	630	100							
150C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	196	1	196	29620	0	4

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	912	0	0	<1
1000	985	0	0	

4.4 S19FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families

CS 129, CS 129L, CS 129AL

This 90 nanometer CMOS Flash technology was introduced in Aug 2006 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three copper layers.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000							
Sample Size	1700	4300	5497	1230							
150C, Zero fails, Process ave. Ea	0	0	0	0	0.7	188	1	188	39317	0	3

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1078	0	0	<1
1000	1155	0	0	

4.5 S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S Product Families

CS 239LS

This 65 nm Mirror bit flash technology was introduced in September 2010 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result						Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)			Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	96	168	1000	2000							
Sample Size	1430	3620	200	5394	1234	90							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0	0.7	69	1	69	15133	0	8

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	2849	0	0	<1
1000	3002	0	0	

4.6 S29GL-T Product Families

CS 340L

This 45nm Mirror bit flash technology was introduced in December 2015 and utilizes a tunnel oxide, Silicon Nitride(SiN) data storage layer, silicided poly word and interconnections are four metal layers with contact plu and five metal layers with contact plug and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000							
Sample Size	1050	2608	3658	527							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	40	1	40	4350	0	26

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	531	0	0	3
1000	453	0	0	

4.7 S25FL1-K, S25FL2-K Product Families

90 nm SPI Floating Gate

90 nm SPI (Serial Peripheral Interface) Floating Gate Flash Technology was introduced in May 2012 and utilizes tunnel oxide, polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000							
Sample Size	1100	3150	4393	1350							
150C, Zero fails, Process ave. Ea	0	0	0	0	0.7	208	1	208	42865	0	3

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	539	0	0	<1
1000	847	0	0	
2000	153	0	0	

4.8 S34ML-1 Product Families

48 nm SLC NAND

48 nm SLC NAND was introduced in July 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 48 nm SLC NAND is using Tungsten.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result						Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)			Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	96	168	1000	2000							
Sample Size	1050	2650	500	4750	1260	100							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0	0.7	74	1	74	15879	0	7

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	604	0	0	<1
1000	604	0	0	

4.9 S34ML-1 Product Families

41 nm SLC NAND

41 nm SLC NAND were introduced in Jun 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 41 nm SLC NAND is using Copper.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result						Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)			Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	96	168	1000	2000							
Sample Size	1100	3200	500	4620	1320	150							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0	0.7	74	1	74	16658	0	7

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1155	0	0	<1
1000	1155	0	0	

4.10 S34ML-2 Product Families

32 nm SLC NAND

32 nm SLC NAND were introduced in October 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 32 nm SLC NAND is using Copper

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result						Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)			Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	96	168	1000	2000							
Sample Size	1370	4137	310	5697	1200	150							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0	0.7	74	1	74	16930	0	7

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1463	0	0	<1
1000	1462	0	0	

4.11 HSLS_USB (CY7C64713* ,CY7C68013A*) Product Families

C8 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	370	370							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	2549	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.12 ASYNC (CY7C1041D*) Product Families

C9 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	152	152							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	1608	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.13 SYNC (CY7C1460K*); HRUSB (CYUSB3304*, CYUSB2302*) Product Families

LL65 Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	71	500	770							
Sample Size		4200		503							
140C, Zero fails, Process ave. Ea		0		0	0.7	110	1	110			
Sample Size	1172		116							0	17
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			
									6543		

4.14 CLOCKS (CY29430F*) Product Families

LP55 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	6074	940							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	6476	0	18

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	239	0	0	23

4.15 ASYNC (CY7C1061AV*, CY7C1041CV33*) Product Families

R7 Technology

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	408	500							
Sample Size	315	236	79							
150C, Zero fails, Process ave. Ea	0	0	0	0.7	170	1	170	2874	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.16 ASYNC (CY62167DV30*) Product Families

R8 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	231	231							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	2444	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.17 SPCM (CY7C144E*) Product Families

R42 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	**1000**							
Sample Size	233	233							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	1605	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.18 SYNC (CY7C1380D*, CY7C1471BV33D*) Product Families

R9 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	178	178							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	1884	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.19 ASYNC (CY62147EV30LL*, CY62167EV18LL*, CY62167EV30LL*) Product Families

R95 Technology

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		154			154							
125C, Zero fails, Process ave. Ea		0			0	0.7	55	1	55			
Sample Size	840		686	154							0	13
150C, Zero fails, Process ave. Ea	0		0	0		0.7	170	1	170			
										8614		

4.20 AUTOPSOC (CY8C21334*, CY8C21534*, CY8C29466*, CY8CTMA120); PSOC (CY8C4124*, CY8C4125*) Product Families

S4 Technology

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	408	1000							
Sample Size	1229		240						0	20
125C, Zero fails, Process ave. Ea	0		0	0.7	55	1	55			
Sample Size		463								
150C, Zero fails, Process ave. Ea		0		0.7	170	1	170	5651		

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	190	0	0	28

4.21 NVSRAM (CY14B101*, CY14B104*, CY14B108L*, CY14B116L*); AUTOPSOC (CY8C20236A*, CY8CTMA461* CY8CTMA616*, CYAT81688*, CY8C4245*); PSOC (CY8C3866A*, CY8C4124, CY8C4125*, CY8C4245*, CY8C4146*, CY8C4246*, CY8C4248*); TYPE-C (CYPD21222*, CYPD21227*, CYPD21228*, CYPD21342*, CYPD3135*, CYPD4226*, CYPD5225); TT (TT21100*, CYTT21403*, CYTT21402*, CYAT81688*, CYTMA445A*); WUSB (CYBL10161*, CYBL10563*) Product Families

S8 Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	408	500	1000							
Sample Size				385							
125C, Zero fails, Process ave. Ea				0	0.7	55	1	55			
Sample Size	101953	1411	8532							10	1
150C, Zero fails, Process ave. Ea	1*	0	0		0.7	170	1	170			
									105121		

Notes:

* *1u (Device: CYPD31357) - Gate Oxide Damage*

- *CAR# 201704039 - CO2:Sparge in the develop rinse limits the incidence of surface charging and gate oxide damage*

Data Retention Bake – 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	1290	0	0	4

4.22 F-RAM (CY15B064*, CY15B102N*, CY15B102Q7*, CY15B104Q7*, CY15B256*, CY15E064J*, FM24C16B7*, FM24V107*, FM24CL64B7*, FM25040B7*, FM25V20A7*, FM25V01*, FM25V107*, FM28V202*) Product Families

130nm TI F-RAM Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	98707	2785							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	19187	0	6

Data Retention Bake – 125/150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000 (125)	1380	0	0	<1
1000 (150)	700	0	0	

4.23 S6AXXXX, S6BXXXX Product Families

180 nm PMICs

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	2469	231	1479	759							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	11120	0	10

4.24 S6J33X, S6J34X Product Families

40 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	4272	2211	1660	401							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	16097	0	7

4.25 S6J31X, S6J32X Product Families

55 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	1288	505	530	253							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	5308	0	22

4.26 S6E1XXX, S6E2XXX, MB9AF11X, MB91F52X Product Families

90 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	4209	792	2493	924							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	17682	0	6

4.27 MB91F4XX, MB95F5XX, MB95F6XX Product Families

180 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000	2000							
Sample Size	3471	2936	535							
125C, Zero fails, Process ave. Ea	0	0	0	0.7	55	1	55	23913	0	5

4.28 MB90F3XX, MB91F3XX, MB95F1XX Product Families

350 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	2060	763	763	534							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	8936	0	13

5. Data Summaries by Package Family

5.1 BGA (Ball Grid Array)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1008	0	0
	264hrs	4120	0	0
High Temperature Storage	1000hrs	6427	0	0
Pressure Cooker Test	96hrs	649	0	0
	168hrs	408	0	0
Temperature Cycle	500cycle	2011	0	0
	1000cycle	7587	0	0
Unbiased HAST	96hrs	4687	0	0
	264hrs	3718	0	0

5.2 BGA (Ball Grid Array) – Flip Chip

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	264hrs	85	0	0
High Temperature Storage	1000hrs	157	0	0
Temperature Cycle	500cycle	159	0	0
	1000cycle	664	0	0

5.3 DFN (Dual Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	613	0	0
High Temperature Storage	1000hrs	708	0	0
Pressure Cooker Test	168hrs	220	0	0
Temperature Cycle	500cycle	749	0	0
	1000cycle	333	0	0
Unbiased HAST	96hrs	361	0	0

5.4 DIP (Dual Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	110	0	0
High Temperature Storage	1000hrs	659	0	0
Pressure Cooker Test	168hrs	472	0	0
Temperature Cycle	500cycle	903	0	0
Unbiased HAST	96hrs	200	0	0

5.5 LCC (Leaded Chip Carrier)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
High Temperature Storage	1000hrs	60	0	0
Pressure Cooker Test	168hrs	60	0	0
Temperature Cycle	500cycle	60	0	0

5.6 LGA (Land grid array)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
High Temperature Storage	1000hrs	90	0	0
Temperature Cycle	1000cycle	462	0	0
Unbiased HAST	264hrs	462	0	0

5.7 QFN (Quad Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	3190	0	0
	264hrs	246	0	0
High Temperature Storage	1000hrs	2560	0	0
Pressure Cooker Test	96hrs	668	0	0
	168hrs	2024	0	0
Temperature Cycle	500cycle	7535	0	0
	1000cycle	25	0	0
Unbiased HAST	96hrs	3297	0	0

5.8 QFP (Quad Flat Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	6481	0	0
High Temperature Storage	1000hrs	6657	0	0
Pressure Cooker Test	96hrs	1006	0	0
	168hrs	891	0	0
Temperature Cycle	500cycle	11726	0	0
	1000cycle	462	0	0
Unbiased HAST	96hrs	8654	0	0

5.9 SOJ (Small Outline J Lead)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	210	0	0
High Temperature Storage	1000hrs	180	0	0
Pressure Cooker Test	168hrs	180	0	0
Temperature Cycle	500cycle	180	0	0

5.10 SOP (Small Outline Gull Wing Lead Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	4450	0	0
	264hrs	231	0	0
High Temperature Storage	1000hrs	4157	4*	962
Pressure Cooker Test	96hrs	1397	0	0
	168hrs	1327	0	0
Temperature Cycle	500cycle	4031	7**	1737
	1000cycle	1918	0	0
Unbiased HAST	96hrs	2307	0	0

Note:
4u (Device: CY2305CSXA, Assy Site: Amkor-Phils (M))*
1u - Lifted Ball
- *CAR# 201529021: Optimized wirebond parameter*

3u – Cut Wedge
- *CAR# 201427001: Implemented new BOM (Bill of Material)*

*7u** (Device: CY2305CSXA, Assy Site: Amkor-Phils (M))*
1u - Lifted Ball
- *CAR# 201529021: Optimized wirebond parameter*

6u - Cut Wedge
- *CAR# 201427001: Implemented new BOM (Bill of Material)*

5.11 SSOP (Shrink Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1469	0	0
High Temperature Storage	1000hrs	960	0	0
Pressure Cooker Test	96hrs	1290	0	0
	168hrs	521	0	0
Temperature Cycle	500cycle	2128	0	0

5.12 TSOP (Thin Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	6242	0	0
	264hrs	693	0	0
High Temperature Storage	1000hrs	7326	0	0
Pressure Cooker Test	96hrs	993	0	0
	168hrs	2276	0	0
Temperature Cycle	500cycle	6227	0	0
	1000cycle	3406	0	0
Unbiased HAST	96hrs	3538	0	0

5.13 WLCSP (Wafer Level Chip Scale Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
High Temperature Storage	1000hrs	694	0	0
Temperature Cycle	1000cycle	1172	0	0
Unbiased HAST	96hrs	1187	0	0
	264hrs	77	0	0

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