2016 Q4 Quarterly Reliability Report

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1. Introduction

Cypress's Reliability Monitor Program (RMP) is used to measure the reliability of all process technologies on a regular basis. This is an extensive effort that is aimed at providing generic fab process coverage for all fab process technologies.

The Reliability Monitor Program has two purposes:

1. Improved Reliability Performance

   Each reject is analyzed to its root cause in order to drive continuous improvement through the implementation of corrective actions.

2. Generation of Reliability Data

   RMP test results are used to assess the benefits of burn-in, provide estimates of typical lifetimes, model field applications, and determine suitability of plastic packaging in various temperature and humidity environments.

A number of process technology groupings are established for the purpose of reliability assessment. These groupings result in larger sample sizes so that the reliability analysis is statistically significant. Process similarity guidelines are used to define these process groupings.

Cypress Semiconductor has established aggressive reliability objectives. The quality standard at Cypress is zero defects, driven by a culture requiring continuous improvement in quality and reliability.

Product reliability is assured by a total quality management system. The quality management system is described in detail in Cypress Semiconductor Quality Manual. Key reliability related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing processes; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking.

Product Reliability data is accumulated as a result of new product qualification test plan activities as well as from the reliability monitor program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Sampling of device is not limited to in-house Cypress facilities but also includes certified external subcontractor foundries.

Reliability strategy requires that every failure that occurs during reliability testing be subjected to failure analysis to determine the failure mechanism. Corrective action is then implemented to prevent future failures, resulting in continuous improvement in product reliability.

Sabbas Daniel

Executive Vice-President, Quality

2. Reliability Tests and Test Conditions

The results of the RMP testing for the past six quarters are summarized in this document. The stress tests employed and the typical test conditions used are shown in the Table 2.1.

Table 2.1 Reliability Monitor Stress Conditions

Stress	Ambient Condition	Typical Read Point
Early Life	150°C, 125°C	48, 96 hours
Inherent Life	150°C, 125°C	168, 408, 500, 1000 hours
Data Retention	150°C, 125°C	1000 hours
HAST	110°C, 85% RH	264 hours
	130°C, 85% RH	96 hours
Temperature Cycle	-40°C to 150°C (Condition M)	1000 cycles
	-55°C to 125°C (Condition B)	1000 cycles
	-65°C to 150°C (Condition C)	500 cycles
Unbiased HAST	110°C, 85% RH, no bias	264 hours
	130°C, 85% RH, no bias	96 hours
Pressure Cooker Test	121°C, 15 PSIG, no bias	96, 168 hours
High Temperature Storage	150°C, 125°C	1000 hours

Package level reliability testing refers to the assessment of the overall reliability of the device in packaged form. This consists of subjecting packaged samples to reliability tests that exposed the sample sets to different stress conditions, after which the samples are tested for any degradation.

At Cypress, plastic surface mount devices are pre-conditioned prior to undergoing Temperature Cycling, Pressure Cooker Test/Unbiased HAST, and HAST. Pre-conditioning per JEDEC Standard JESD22-A113 is required in order to simulate the stresses to which the packaged parts are subjected to during shipping, storage, board assembly and cleaning operations. Package reliability tests are performed as part of the qualification processes and as part of the standard reliability monitor program. The reliability test employed is chosen based on the failure mechanism, as different stress tests accelerate different failure mechanisms. These reliability tests utilize one or more of the following stress factors such as: temperature, moisture or humidity, voltage and pressure, to accelerate failure. Figure 2.1 shows Cypress package reliability stress flow. Packages are soaked and reflowed based on their shipping moisture sensitivity classification. The samples are tested (acoustic and electrical) after preconditioning, failures from which are considered as preconditioning failures and not reliability failures. Preconditioning failures should be taken seriously, since these imply that the samples are not robust enough to withstand the board mounting process.

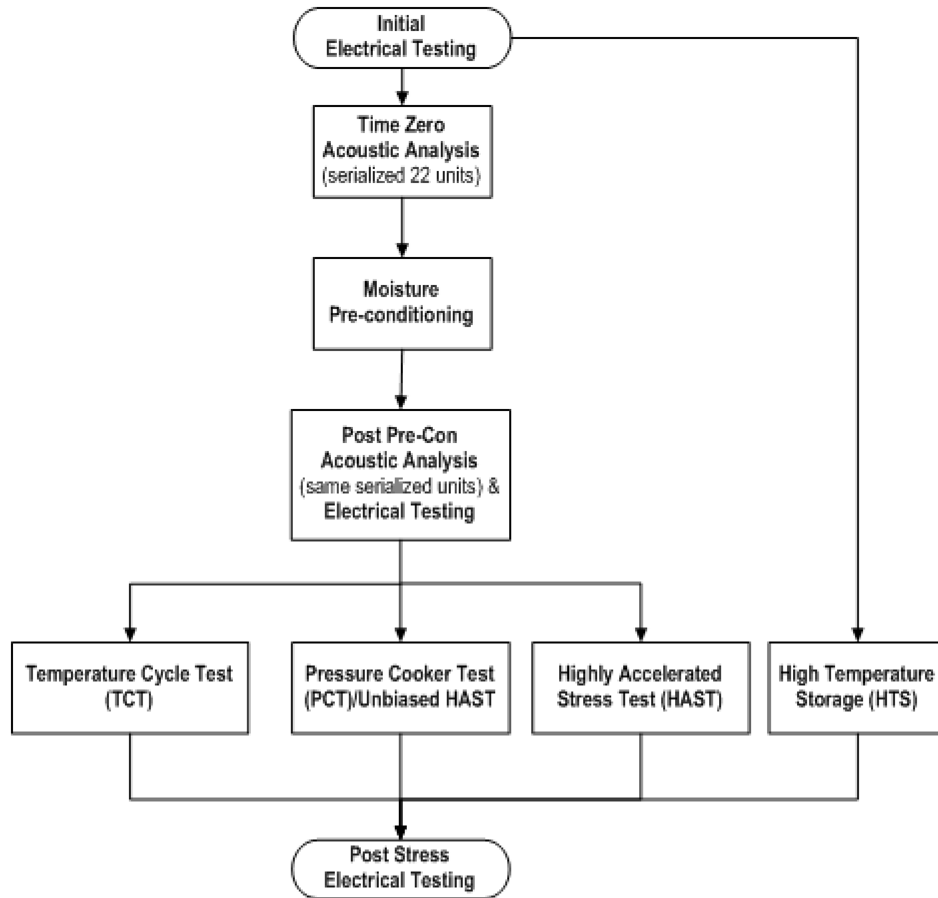


Figure 2.1 Cypress Package Reliability Stress Flow

3. Reliability Data/Analysis

The reliability data generated from the Reliability monitor Program is presented in this section along with a detailed description of the modeling procedure used for estimating reliability under field conditions.
Also included is a summary of environmental stress results for each process technology grouping by package types.

3.1 The Exponential Distribution

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. No actual distribution can be implied as there is seldom enough data to determine one. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant.

The exponential distribution is the only one for which a MTTF (mean time to failure) value may easily be estimated and it is simply the reciprocal of the failure rate (λ). In addition it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The conventional expression for the failure rate, λ, is

$$\lambda = \chi^2(2n + 2, 1 - \alpha)*10^9/(2*SS*t*AF)$$

where λ is the failure rate in FITs (failures per billion unit-hours), $\chi^2(2n+2,1-\alpha)/2$ is the upper confidence value for "**n**" failures and upper confidence limit, (expressed as a decimal value), **SS** is the sample size, t is the test duration in hours, and **AF** is the acceleration factor relating the life test junction temperature to a assumed field junction temperature.

The χ^2(chi square) value for 2n+2 degrees of freedom and the probability, 1-α, can be obtained from a table or calculated using Microsoft® Excel chi squared inverse function [=CHIINV(1-α,2n+2)].

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-part sample from a certain product population had one failure and a 60% confidence level was desired. The chi square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the "true" value of the population's defect rate is between zero (or some very small value) and 2.02%.

3.2 Failure Distributions

The lognormal and Weibull CDF's are the distributions most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The lognormal distribution is specified by two parameters: T_{50}, the median time to failure, and sigma, the shape parameter. Similarly, the Weibull distribution, which can be written in closed form as

$$F(t) = 1 - \exp[-(t/c)^m],$$

is characterized by a characteristic life c and a shape parameter m. The value of the shape parameter determines whether the failure rate is increasing (m>1), decreasing (m<1), or constant (m=1). The exponential distribution, is specified completely by the one parameter c which is called the mean time to failure (MTTF). Figures 1 and 2 show failure rates for several values of the scale parameters of the lognormal and Weibull distributions, respectively.

$$F(t) = 1 - \exp[-(t/c)],$$

Figure 1. Lognormal Distribution

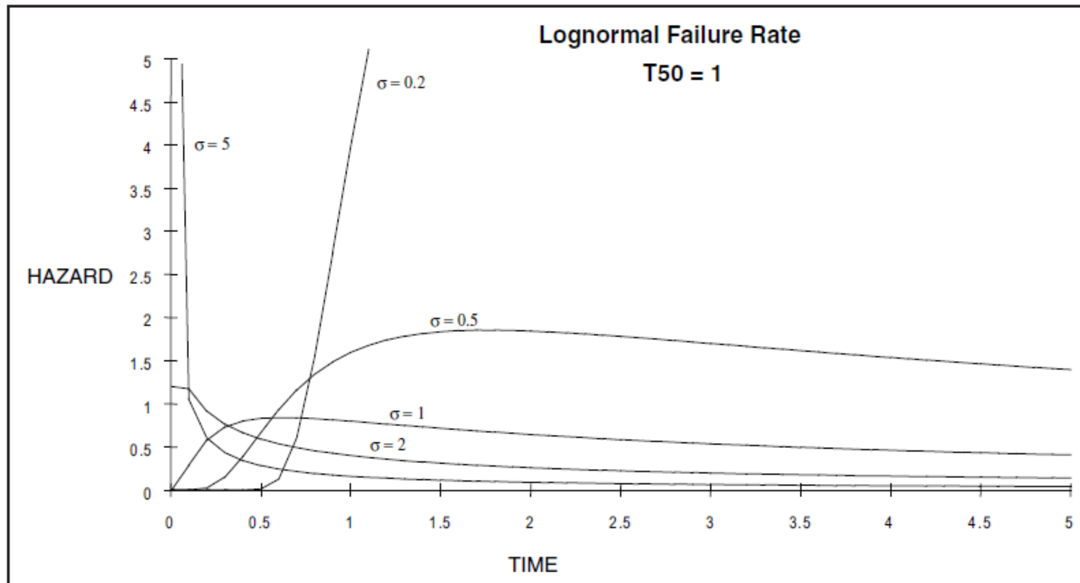
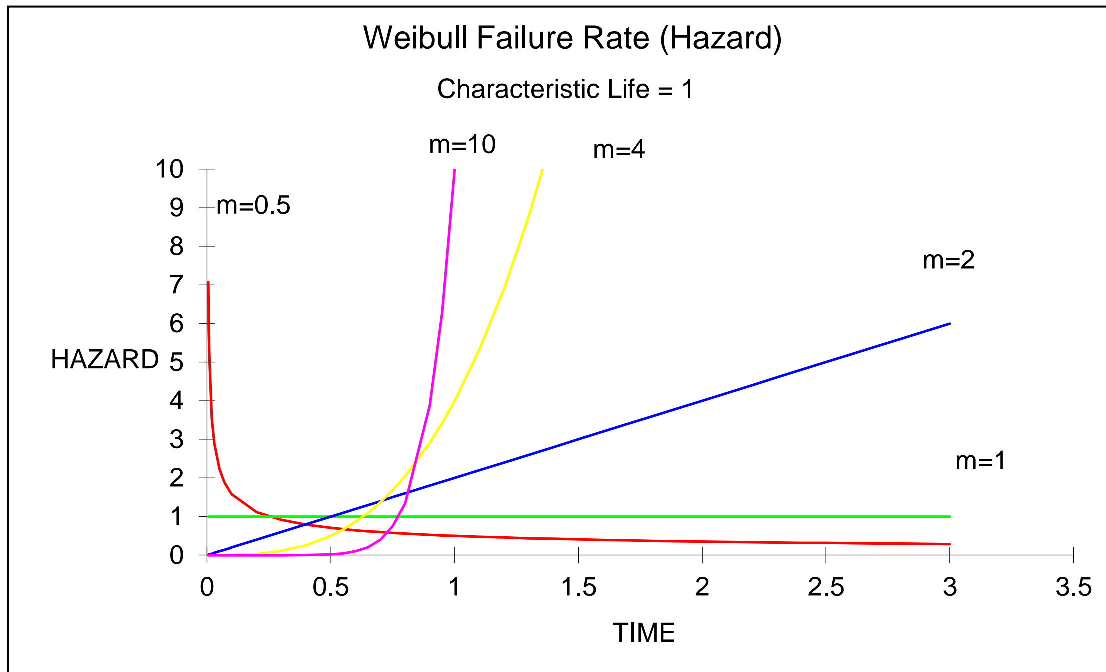


Figure 2. Weibull Distribution



3.3 Calculations of Failure Rates

To estimate field failure rates from reliability studies, many factors must be considered. One primary requirement is the identification of individual failure mechanisms in order to ascribe the failures to the proper categories used in the Cypress reliability model.

3.3.1 Considerations and Assumptions

1. Defective subpopulations and Early Life failures:

   In any production lot a defective subpopulation may exist. These are devices that fail by a mechanism that is not common to the general population and is usually the result of some processing error or defect. These failures usually occurs early and consequently called Early Life failures. Early life reliability is reported in terms of ppm defective expected during the first year of use under typical use conditions. No upper confidence bound will be used for this estimate. The ppm defective is the ration of the number of rejects to the number of samples and expressed in ppm.

   PPM = (Total Reject / Total samples) * 1,000,000

2. Inherent Life failures:

   Failures that occur in later life reliability are usually caused by mechanisms related to defects that could occur in any product of this type. These are known here as Inherent Life failures. Inherent life reliability is reported in using the exponential model, in terms of FITs (failures per billion unit-hours) with a 60% upper confidence bound for zero failure.

3. Estimation of thermal acceleration factors:

   The best-known activation energies for each mechanism are used in calculating the thermal acceleration using the standard Arrhenius equation for thermal acceleration. For each process group/ package combination, representative acceleration factors were estimated based on the weighted average of acceleration factors of individual devices in that group.

4. Voltage acceleration factor is not included in failure rate calculation even though voltage acceleration may be used during stress.

5. It is common in reliability literature to see failure rates stated at a specified level of confidence:

   For example, a 60% upper confidence limit on the failure rate indicates that unless a 4 in 10 chance (40%) has occurred, the true population failure rate is less than the stated limit. The summation of individual failure rate components, each at 60% confidence, will however, result in an overall failure rate at an unknown confidence level that may dramatically exceed 60%.The failure rates quoted in the Quarterly Reliability Report are at a 60% upper confidence level.

4. Data Summaries by Process Technology

4.1. S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families

CS 69S, CS 69LS

This 0.11 micron CMOS Flash technology was introduced in December 2003 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	6679	150	8096	1800	60							
150C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	217	1	217	73724	0	2

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1889	0	0	<1
1000	1883	0	0	
2000	824	0	0	

4.2. S29AL-J, S29AS-J, S29JL-J Product Families

CS 69SS, CS 69LSS

This 0.11 micron CMOS Flash technology was introduced in February 2008 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	6400	600	6049	2220	160							
150C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	227	1	227	81502	0	1

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1958	0	0	<1
1000	1958	0	0	
2000	981	0	0	

4.3. S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL-N, S71WS-N Product Families

CS 119S, CS 119LS

This 0.11 micron CMOS Flash technology was introduced in June 2004 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three or four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	3950	3788	4549	1250	100							
150C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	196	1	196	43516	0	3

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	2097	0	0	<1
1000	1946	0	0	

4.4. S19FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families

CS 129, CS 129L, CS 129AL

This 90 nanometer CMOS Flash technology was introduced in Aug 2006 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three copper layers.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	168	1000							
Sample Size	6580	6579	840							
150C, Zero fails, Process ave. Ea	0	0	0	0.7	188	1	188	38459	0	3

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	2002	0	0	<1
1000	1925	0	0	

4.5. S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S Product Families

CS 239LS

This 65 nm Mirror bit flash technology was introduced in September 2010 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	5660	3970	5563	1542	135							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	69	1	69	19036	0	6

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	4215	0	0	<1
1000	3893	0	0	

4.6. S25FL1-K, S25FL2-K Product Families

90 nm SPI Floating Gate

90 nm SPI (Serial Peripheral Interface) Floating Gate Flash Technology was introduced in May 2012 and utilizes tunnel oxide, polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	168	1000							
Sample Size	4900	4296	1440							
150C, Zero fails, Process ave. Ea	0	0	0	0.7	208	1	208	47186	0	2

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1001	0	0	<1
1000	1000	0	0	

4.7. S34ML-1 Product Families

48 nm SLC NAND

48 nm SLC NAND was introduced in July 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 48 nm SLC NAND is using Tungsten.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	6100	1050	6499	2040	100							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	74	1	74	25256	0	5

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	1950	0	0	<1
1000	1950	0	0	

4.8. S34ML-1 Product Families

41 nm SLC NAND

41 nm SLC NAND were introduced in Jun 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 41 nm SLC NAND is using Copper.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	6200	1100	6600	2160	100							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	74	1	74	26313	0	4

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	2420	0	0	<1
1000	2189	0	0	

4.9. S34ML-2 Product Families

32 nm SLC NAND

32 nm SLC NAND were introduced in October 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 32 nm SLC NAND is using Copper

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	24	48	168	1000	2000							
Sample Size	7310	990	7500	2400	150							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	74	1	74	29776	0	4

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	2805	0	0	<1
1000	2648	0	0	

4.10. WUSB (CYRF6936*) Product Families

B53 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	231	231							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	**	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.11. HS_USB (CY7C65630*) Product Families

C8 Technology

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	408	1000							
Sample Size	2367								0	12
125C, Zero fails, Process ave. Ea	0									
Sample Size		231	359							
150C, Zero fails, Process ave. Ea		0	0	0.7	170	1	170	9592		

4.12. FAST (CY7C1041D*) Product Families

C9 Technology

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500							
Sample Size		77	77						0	**
125C, Zero fails, Process ave. Ea		0	0	0.7	55	1	55			
Sample Size	308		308							
150C, Zero fails, Process ave. Ea	0		0	0.7	170	1	170	**		

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.13. FAST (CY7C1041/61G*, CY62147/67G*), SYNC (CY7C1370K*, CY7C1441K*, CY7C1460/61K*) Product Families

LL65 Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500	1000							
Sample Size		35100	587	1582							
125C, Zero fails, Process ave. Ea		0	0	0	0.7	55	1	55		0	8
Sample Size	3921		196								
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170	14995		

4.14. Clocks (CY29430F) Product Families

LP55 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	3039	548							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55		0	11
Sample Size		319							
150C, Zero fails, Process ave. Ea		0	0.7	70	1	170	10527		

4.15. HRBuffer (CY2305C) Product Families

R52 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	408							
Sample Size	2399	160							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	**	0	**

Note:

***Insufficient data – interpret as insufficient accumulated life-time hours to project a 60%confidence bound for a zero-fails sample.*

4.16. HRFAST (CY7C1019C*, CY7C1021C*, CY7C1041C) Product Families

R7 Technology

Failure Mechanisms	Read Point / Test Result			Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	408	500							
Sample Size	2394	391	300							
150C, Zero fails, Process ave. Ea	0	0	0	0.7	170	1	170	6551	0	17

4.17. SYNC (CY7C1370D*, CY7C1380D*, CY7C1381D*) Product Families

R9 Technology

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	6516	355							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	3757	0	30

4.18. HRMPWR (CY62137F*, CY62128/46/47E*), MICROPWR (CY62147/57/67E*) Product Families

R95 Technology

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	168	408	1000							
Sample Size	501		231		270							
125C, Zero fails, Process ave. Ea	0		0		0	0.7	55	1	55			
Sample Size		384		384								
150C, Zero fails, Process ave. Ea		0		0		0.7	170	1	170	5443	0	21

4.19. CAPS (CY8C21534*), HRPSOC (CY8C24894*, CY8CTMA120*, CY8C22345*), LS_USB (CY7C64215*) Product Families

S4 Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500	1000							
Sample Size		6271		783							
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	3020		308							0	13
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			
									8654		

4.20. CAPS(CY8C20236/20467*/CYTT21402*/4032*/CY8CTMA445*/CY8CTST242*); HRPSOC (CY8C4125/4245P*/4247A*, CYONSFN3050A*, CY8CTMA616A*, CYAT81688*); NVP (CY14V101P, CY14B101L/104N*), PSOC (CY8C4045A*/4128*/4146A*/42452A*/4246P*/4248A*/CY8CMBR3106*/3108*/31552*); TT (CYTMA450*), TYPE-C (CYPD21342*/4125*/4225*); WUSB (CYBL10462*/561*/563*, CYRF6936) Product Families

S8 Technology

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		4666			175							
125C, Zero fails, Process ave. Ea		1**			0	0.7	55	1	55			
Sample Size	122720		946	4011							24	2
150C, Zero fails, Process ave. Ea	2*		0	0		0.7	170	1	170			
										51818		

Notes:

** 2u (Devices: CYTMA450/CYAT816882) - Non Visual Defect (NVD)*

- Will be covered by Fab's continuous defect improvement

*** 1u (Device: CYBL10563) - Wire to Wire Short*

- CAR# 201530013: Optimized wirebond layout

Data Retention Bake – 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	160	0	0	2
1000	2159	0	0	

4.21. F-RAM (CY15B102/104Q*, FM25V20A*, FM25CL64B) Product Families

130nm TI F-RAM Technology

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	168	1000							
Sample Size	2000	8840	236	705							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	5130	0	22

Data Retention Bake – 125/150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000 (125)	480	0	0	<1
1000 (150)	80	0	0	

4.22. S6AP, S6BP, S6AE Product Families

180 nm PMICs

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500	1000	2000							
Sample Size	2717	2490	1040	1049	244							
125C, Zero fails, Process ave. Ea	0	0	0	0	0	0.7	55	1	55		0	13
Totals										8877		

4.23. S6J3 Product Families

55 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500	1000	2000							
Sample Size	2400	799	799	261							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	7303	0	16

4.24. S6E2, MB9AF, MB91F Product Families

90 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	10050	1847	1847	394							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	15439	0	7

4.25. MB91, MB96 Product Families

180 nm MCU (FLASH)

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	500	1000	2000							
Sample Size	6425	1723	1723	544							
125C, Zero fails, Process ave. Ea	0	0	0	0	0.7	55	1	55	15619	0	7

5. Data Summaries by Package Family

5.1 BGA (Ball Grid Array)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	2259	0	0
	264 hrs	5716	0	0
High Temperature Storage	1000 hrs	10160	0	0
Pressure Cooker Test	96 hrs	1709	0	0
	168 hrs	2238	0	0
Temperature Cycle	500 cycles	5395	0	0
	1000 cycles	6679	0	0
Unbiased HAST	96 hrs	5774	0	0
	264 hrs	933	0	0

5.2 BGA (Ball Grid Array) – Flip Chip

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	58	0	0
	264 hrs	114	0	0
High Temperature Storage	1000 hrs	317	0	0
Pressure Cooker Test	96 hrs	158	0	0
Temperature Cycle	500 cycles	238	0	0
	1000 cycles	797	0	0

5.3 DFN (Dual Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	743	0	0
	128 hrs	28	0	0
High Temperature Storage	1000 hrs	514	0	0
Pressure Cooker Test	168 hrs	459	0	0
Temperature Cycle	500 cycles	1056	0	0
	1000 cycles	616	0	0
Unbiased HAST	96 hrs	694	0	0

5.4 DIP (Dual Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	240	0	0
High Temperature Storage	1000 hrs	378	0	0
Pressure Cooker Test	168 hrs	720	1*	1389
Temperature Cycle	500 cycles	829	0	0
Unbiased HAST	96 hrs	50	0	0

Note:
**1u (Device: CS6632AF, Assy Site: CML-RA) - Lifted Ball*
- *CAR# 201542014: Optimized wirebond parameter*

5.5 LCC (Leaded Chip Carrier)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
High Temperature Storage	1000 hrs	60	0	0
Pressure Cooker Test	168 hrs	29	0	0
Temperature Cycle	500 cycles	30	0	0

5.6 QFN (Quad Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	2592	0	0
	264 hrs	830	0	0
High Temperature Storage	1000 hrs	3027	0	0
Pressure Cooker Test	96 hrs	599	0	0
	168 hrs	3145	0	0
Temperature Cycle	500 cycles	8043	0	0
Unbiased HAST	96 hrs	1925	0	0
	264 hrs	22	0	0

5.7 QFP (Quad Flat Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	4330	0	0
High Temperature Storage	1000 hrs	3884	0	0
Pressure Cooker Test	96 hrs	975	0	0
	168 hrs	2511	0	0
Temperature Cycle	500 cycles	8202	0	0
	1000 cycles	462	0	0
Unbiased HAST	96 hrs	4923	0	0

5.8 SOJ (Small Outline J Lead)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	167	0	0
High Temperature Storage	1000 hrs	240	0	0
Pressure Cooker Test	168 hrs	308	0	0
Temperature Cycle	500 cycles	340	0	0

5.9 SOP (Small Outline Gull Wing Lead Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	5386	0	0
	264 hrs	231	0	0
High Temperature Storage	1000 hrs	5446	5*	918
Pressure Cooker Test	96 hrs	778	0	0
	168 hrs	2678	0	0
Temperature Cycle	500 cycles	4539	7**	1542
	1000 cycles	2924	0	0
Unbiased HAST	96 hrs	3158	0	0

Note:
5u (Device: CY2305CSXA, Assy Site: Amkor-Phils (M))*
2u - Lifted Ball
- *CAR# 201529021: Optimized wirebond parameter*

3u – Cut Wedge
- *CAR# 201427001: Implemented new BOM (Bill of Material)*

*7u** (Device: CY2305CSXA, Assy Site: Amkor-Phils (M))*
1u - Lifted Ball
- *CAR# 201529021: Optimized wirebond parameter*

6u - Cut Wedge
- *CAR# 201427001: Implemented new BOM (Bill of Material)*

5.10 SSOP (Shrink Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	480	0	0
	128 hrs	77	0	0
High Temperature Storage	1000 hrs	826	0	0
Pressure Cooker Test	96 hrs	210	0	0
	168 hrs	629	0	0
Temperature Cycle	500 cycles	1385	0	0

5.11 TSOP (Thin Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	8026	9*	1121
	128 hrs	77	0	0
	264 hrs	462	0	0
High Temperature Storage	1000 hrs	11722	0	0
Pressure Cooker Test	96 hrs	1124	0	0
	168 hrs	1677	0	0
Temperature Cycle	500 cycles	5136	0	0
	1000 cycles	5400	0	0
Unbiased HAST	96 hrs	6398	0	0

Note:
**9u (Device: CY62167ELL, Assy Site: ASE-Taiwan (G)) - Lifted Ball*
- *CAR# 201611019: Optimized wirebond parameter*

5.12 WLCSP (Wafer Level Chip Scale Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96 hrs	60	0	0
	264 hrs	79	0	0
High Temperature Storage	1000 hrs	235	0	0
Pressure Cooker Test	96 hrs	628	0	0
	168 hrs	28	0	0
Temperature Cycle	1000 cycles	1156	0	0
Unbiased HAST	96 hrs	658	0	0
	264 hrs	77	0	0

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Rev.	ECN No.	Orig. of Change	Description of Change
**	5559019	BHGO	Initial Spec Release
*A	5690099	BHGO DCon	Corrected the Data Retention Bake Temperature from 125C to 150C at page 13, 15, 16, 17. Replaced CY logo