Thermal Conditions and Parameters

AN201006 discusses the thermal considerations and parameters when using SkyHigh devices in printed wiring board (PWB) geometrics.

1 Introduction

As printed circuit board (PWB) designs become more complex and available space gets smaller, managing heat during assembly becomes increasingly important. Even though SkyHighMemory products usually use little power, nearby high-power devices can cause significant local heating. This application note provides some key thermal parameters definition and a straightforward methodology for computing the junction temperature of SkyHighMemory products.

2 General

Mathematical, experimental, and numerical techniques used to model and predict the thermal state of a particular system are governed by the JESD51 family of specifications. Specific thermal models (outside the scope of this application note) are governed by the JESD51 family of specifications. Although thermal analyses have been in use for several decades, the associated techniques and methodologies are not evolving at the same rate as the number of new packages and technologies are expanding. As a result, some of the information might be outdated and sometimes may mislead the reader. This application note is intended to summarize the key factors and mathematical parameters used in thermal analysis and to explain it in a manner that is both useful and straightforward.

3 Terms and definitions

The thermal resistance of a semiconductor device is generally defined as:

$$\theta_{JX} = \frac{T_J - T_X}{P_H} \quad \ldots (1)$$

- θ_{JX} = thermal resistance from device junction to a specific environment [°C/W]
- T_J = device junction temperature in the steady state test condition [°C]
- T_X = reference temperature for the specific environment [°C]
- P_H = power dissipated in the device [W]
- Common reference temperatures (X) are as follows:
- T_A = reference temperature for the ambient environment, measured approximately three inches (7.62 cm) from the package
- T_B = reference temperature for the board, measured on or near a ball or lead of the package
- T_C = reference temperature for the top of the package, measured directly in the center.

The primary consideration for the functionality and reliability of SkyHighMemory products is T_J the junction temperature. This document includes an overview of junction temperature parameters based on the product families. It is essential that each device operates below the defined junction temperature to ensure proper functionality and long-term reliability of the device.

4 Device Thermal Resistance Model and parameters

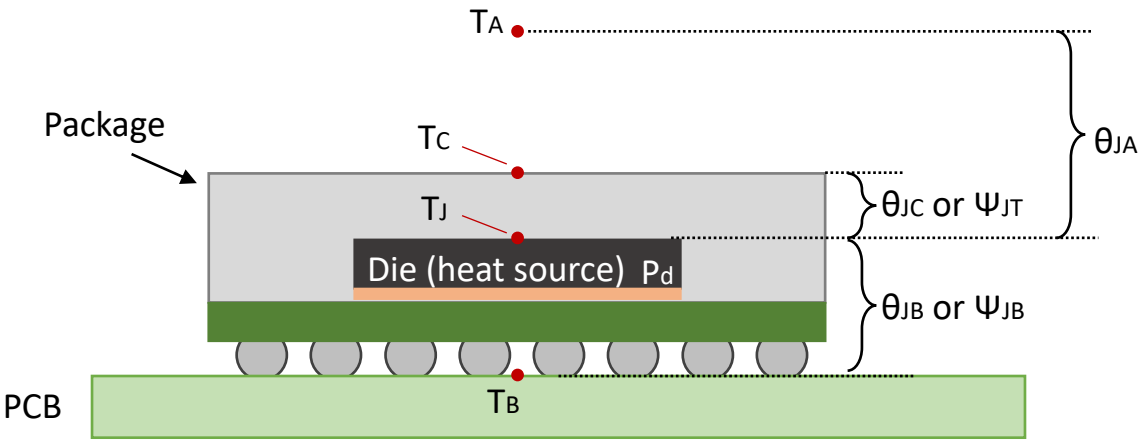

Figure 1: Model of Device Thermal Resistance Parameters

T_A	Temperature at Ambient air	Unit
T_J	Temperature at Junction of device	ºC
T_C	Temperature of Case	ºC
T_B	Temperature of Board	ºC
P_d	Power Dissipation of the Device. P_D = I * V	W
T_{JMAX}	Junction Temperature Max. The spec that T_J must not exceed.	ºC
θ_{JA}	Theta JA. Thermal Resistance Junction-to-Ambient	ºC/W
θ_{JB}	Theta JB. Thermal Resistance junction-to-Board	ºC/W
θ_{JC}	Theta JC. Thermal Resistance Junction-to-Case	ºC/W
ψ_{JB}	Psi JB. Junction-to-Board characterization parameter	ºC/W
ψ_{JT}	Psi JT. Junction-to-Top (of package) characterization parameter	ºC/W

Table 1: Thermal Resistance / Characterization Parameters

SkyHighMemory reliability reports provide the above thermal / Characterization parameter for each product except T_A, P_d which depends on customer usage. T_{JMAX} is defined for some products, listed in this document and is defined as a reference data for device max power.

The parameters θ_{JC} / θ_{JB} and ψ_{JT} /ψ_{JB} have similar definitions and depends on the package/system type:

- θJC / θJB is recommended for ceramic or hermetic package with heat sink that provides sufficient cooling usage.
- ψJT /ψJB is recommended for plastic package with still air usage.

The latter is recommended for SkyHighMemory product since all of them are plastic-package and have low heat dissipation.

5 Device TJMAX

SkyHighMemory defines TJMAX for eMMC devices. No definitions are defined for SLC ONFI NAND, SPI NAND and MCP (SLC+DRAM) products since they are not power devices. No heat dissipation is expected.

Product	Operation Temperature(°C)	T_{JMAX} (°C)
eMMC Product	Wireless -25 to +85	90
	Industrial -40 to 85	100
	Automotive -40 to +85	100
	Automotive Extended -40 to +105	110
SLC ONFI NAND	–	No definition
SPI NAND	–	No definition
MCP (SLC NAND + DRAM)	–	No definition

Table 2: Maximum Junction Temperature

6 Thermal Estimation

Calculating Tj in ideal condition

Assume the conditions with no localized heating, for a typical BGA package and product, the following formula is known,

$$\theta_{JA} = \frac{T_J - T_A}{P_d}$$

$$T_J = T_A + (\theta_{JA} \times P_d) \quad \ldots (2) \; {}^*P_d = I \times V$$

For the device where T_{AMAX} is specified, Thermal design should ensure that T_J does not exceed T_{JMAX}

Enter the ψJT parameter

$$\psi_{JT} = \frac{T_J - T_C}{P_d}$$

In here, T_C can be estimated as follows,

$$T_C = T_J - (\psi_{JT} \times P_d)$$

$$T_C = T_A + (\theta_{JA} \times P_d) - (\psi_{JT} \times P_d)$$

On the other hand, the case temperature can be measured by attaching a thermocouple to the top center of the component. TJ can be estimated as follows,

$$T_J = T_C + (\psi_{JT} \times P_d) \ldots (3)$$

For the device where T_{AMAX} is specified, Thermal design should ensure that T_J does not exceed T_{JMAX}.

This method is preferred over Equation (2) for complex models, such as other heat sources on the board.

Note: Board temperature estimation is not discussed here because the customer environment and the influence of other heat-generating devices are more relevant to this document.

7 Conclusion

This application note clarifies the origin and use of various thermal parameters and provides a straightforward methodology for computing the junction temperature. By using these techniques and computations, a more accurate calculation of critical thermal temperatures can be done, and a better understanding of relevant thermal issues can be achieved.

8 References

JESD51, Methodology for the Thermal Measurement of Component Packages
JESD51-1, Integrated Circuit Thermal Measurement Method - Electrical Test Method
JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-4, Thermal Test Chip Guideline (Wire Bond Type Chip)
JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Document History Page

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