Qualification Report of Nickel/Palladium/Gold-Finish for Integrated Circuits

Cypress Semiconductor
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1.0 INTRODUCTION

Cypress's roadmap to Palladium (Pd) – based lead finish for assembled leadframe packages is motivated by the semiconductor and electronics industries' requirement of lead-free in electronic packaging. Lead (Pb) as an alloying element in solders has resulted in environmental concerns due to potential toxicity. Therefore various legislations to ban lead are being driven worldwide.

European Council Directive on Waste from Electrical and Electronic Equipment (WEEE) proposes restrictions on the use of Pb, among other materials, in electronic products. In April of 1997, the Japanese Ministry of International Trade and Industry set numerical target for the amount of Pb used for automobiles, except for batteries, and later ordered that it be reduced "to half compared to 1996 by the end of 2000 and to one third by the end of 2005". The US EPA announced on July 29,1999 a proposed rule to drastically lower reporting thresholds for Pb and Pb compounds to the Toxic Release Inventory from 10,000 lbs. to 10 lbs.

Cypress is committed to working with its customers to offer lead-free packaging solutions. There are several options in approaching Pb-free lead finish packaging. For instance, Cypress subcontractors are offering Tin-based lead-free lead finish while Cypress in-house manufacturing is Palladium-based lead finish solution. During its initial phase, Cypress will focus on in-house manufacturing operation.

There are two paths to a lead-free solder joint in electronics manufacturing. First is elimination of Lead (Pb) in component lead finish and secondly is eliminating Lead (Pb) in solder pastes used on printed wiring board (PWB). Lead-free solder paste usually requires higher reflow temperatures, typically 245-260 ^{0}C. At present, the electronics industry is still developing packaging materials capable of meeting the higher reflow temperature requirements.

Cypress in-house manufacturing strategy is to offer its customers Palladium – based lead finish as a first phase. This would entail no changes with customer's existing lines, since Palladium–based lead finish will have the same reflow processing as Tin/Lead (Sn/Pb) components; i.e. 220 ^{0}C. The second phase is to improve package thermal robustness with Palladium-based lead finish to enable the higher reflow temperature compatibility required for Pb-free solder pastes at maximum 260 ^{0}C.

2.0 CYPRESS Pd-BASED LEAD FINISH STRUCTURE & COMPOSITION

There are several Palladium-based lead finishes in view of metal layers and its composition. Texas Instruments, for example, has a long and successful history with its Four-Layer Ni/Pd. They recently have introduced a Three-Layer Ni/Pd/Au Finish structure because of its improved solderability performance. Extensive studies show that Ni/Pd/Au finished components have excellent performance with both Pb-based and Pb-free based solder paste. Also, wetting balance tests show excellent wetting time for Ni/Pd/Au-finished leads versus Ni/Pd and Sn/Pb finished leads. Faster wetting times in solderability tests typically indicate improved wetting with the variety of Pb-free solder alloys.

Cypress Pd-based lead finish structure is Three-Layer Ni/Pd/Au. Thickness of Nickel (Ni) ranges from 20 – 80 *u*inch, Palladium (Pd) at 0.8 *u*inch minimum and Gold (Au) flash of 0.12 – 0.6 *u*inch. Cypress is also performing extensive engineering studies to reduce Palladium thickness to 0.2 *u*inch minimum. This will be on-line in either our Phase II or Phase III plans.

3.0 COMPONENT RELIBILITY QUALIFICATION

Requirements for component reliability qualification are per Cypress Specification 25-00112 “Qualification Test Plan”. So far, the completed qualifications with Cypress Ni/Pd/Au-finish IC packages are outlined below.

3.1 Summary of Package Qualifications

Cypress QTP Number	Qual Description	Qual Level MSL + Reflow
015108	SOIC 20/24L Ni/Pd/Au Finish	MSL1, 235 degC
010612	SOIC 20/24L Ni/Pd/Au Finish	MSL1, 220 degC
013805	SSOP 48/56L Ni/Pd/Au Finish	MSL1, 235 degC
013802	TSSOP 16/20L Ni/Pd/Au Finish	MSL1, 235 degC
015107	TSSOP 16/20L Ni/Pd/Au Finish	MSL1, 260 degC

3.2 Summary of Package Reliability Tests

3.2.1 Acoustic Monitor Stress (C-SAM)

Test Vehicle	Before MSL1 Pre-con				After MSL1 Pre-con				Result
	Die Top	Lead finger	Paddle Bottom	External Visual	Die Top	Lead finger	Paddle Bottom	External Visual	
TV1	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	Passed
TV2	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	Passed
TV3	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	Passed

3.2.2 Moisture Preconditioning (MSL1)

Test Vehicle	Electrical Test Results	Remarks
TV1	0/150	Passed
TV2	0/50	Passed
TV3	0/50	Passed

3.2.3 Pressure Cooker Test (PCT)

Test Vehicle	Electrical Test Results	Remarks
TV1	0/50	Passed

3.2.4 Temperature Cycle Test (TC)

Test Vehicle	Electrical Test Results (after 300 cycles)	Remarks
TV1	0/50	Passed
TV2	0/50	Passed
TV3	0/50	Passed

3.2.5 Highly Accelerated Stress Test (HAST)

Test Vehicle	Electrical Test Results	Remarks
TV1	0/50	Passed

4.0 COMPONENT SOLDERABILITY TEST DATA

Solderability testing was done to evaluate the performance of the component in board mounting operation. It is done based on IPC/EIA J-STD-002A standards. Solderability test method is Ceramic Plate Test (CPT), which simulates the board mount reflow environment for surface mounting package family.

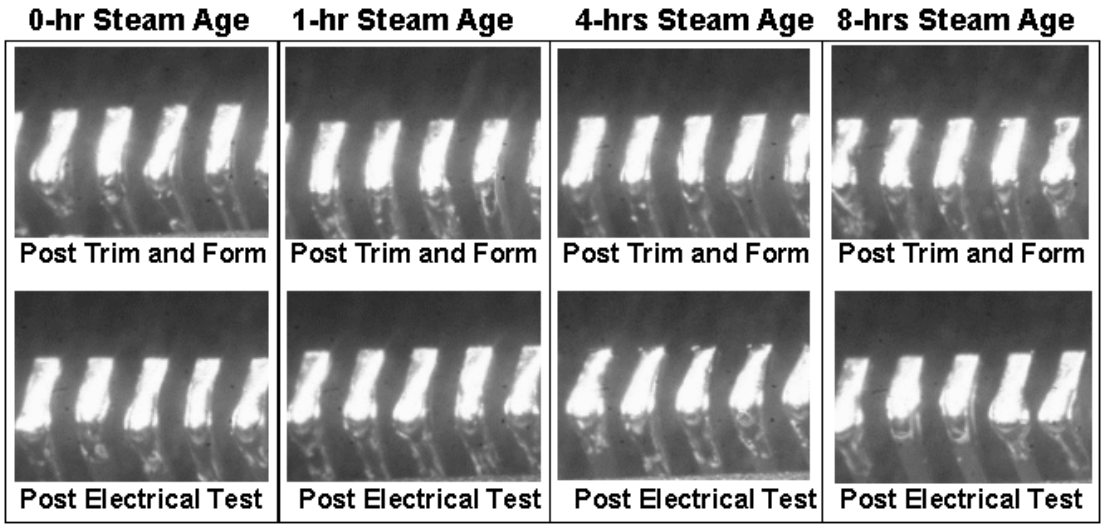
4.1 Test Procedures

1. Component to be tested (Both post trim-form and post electrical test) are steam-aged at 93^{o}C temperature for 0-hour, 1-hour, 4-hours, and 8-hours duration.
2. Solder paste with Sn63/Pb37 solder alloy and RMA flux type is printed onto a ceramic plate using solder stencil. The paste print is equal to the pattern of the leads to be tested.
3. The component leads are then placed onto the solder paste print on the ceramic plate.
4. The ceramic plate is processed through a reflow cycle and then allowed to cool.
5. After reflow, the component is removed from the ceramic plate and cleaned for flux residue.
6. The component leads are then inspected per solderability inspection criteria.

4.2 Solderability Test Data with various steam age time

Steam-age Duration	Steam-age Temperature	Lead Visual Inspection (Reject/Sample size)
0 hr	93 ^{o}C	0/2
1 hr	93 ^{o}C	0/2
4 hrs	93 ^{o}C	0/2
8 hrs	93 ^{o}C	0/6

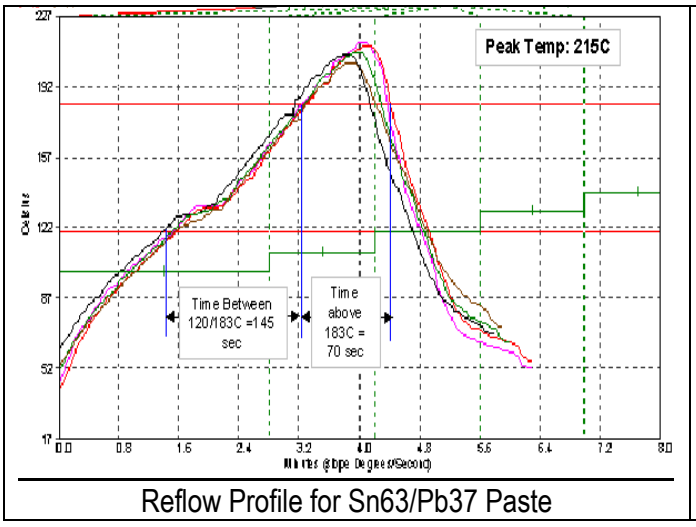
4.3 Visual Appearance of Leads after Solderability



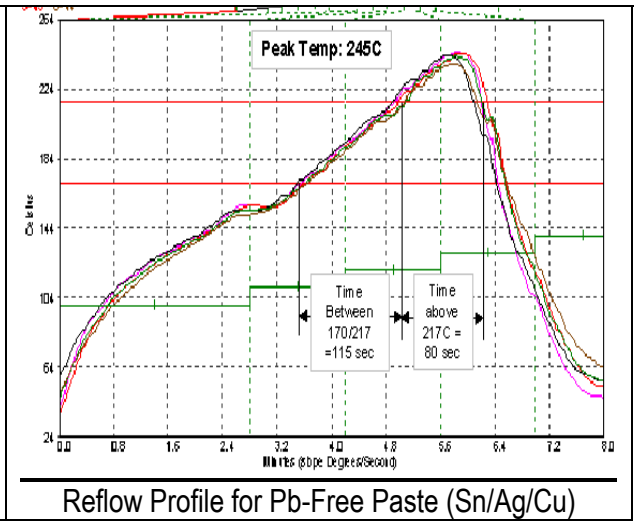
5.0 ACTUAL BOARD MOUNT DATA

Actual board mounting evaluation was performed for Cypress components by Solectron, Milpitas, CA. Standard Sn/Pb plated components and Ni/Pd/Au plated components were evaluated with Sn/Pb solder paste and Pb-free Sn/Ag/Cu paste flow. Same profiles were applied for both Sn-Pb plated components and Ni/Pd/Au plated ones.

5.1 Reflow Profile



Reflow Profile for Sn63/Pb37 Paste

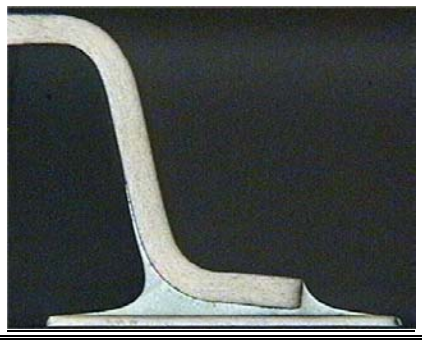
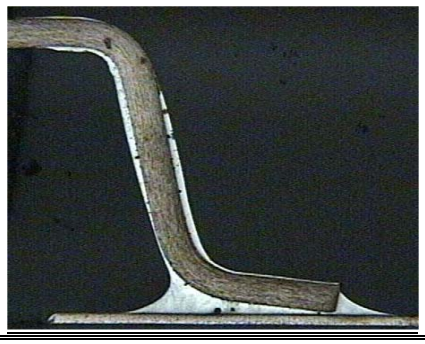
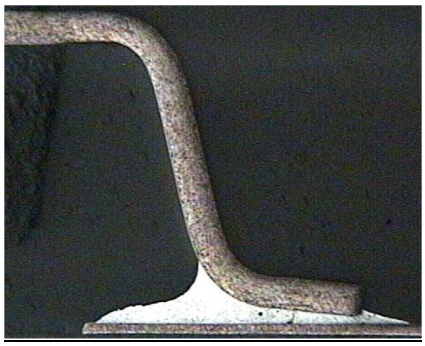
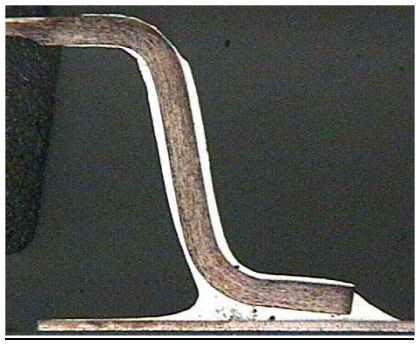


Reflow Profile for Pb-Free Paste (Sn/Ag/Cu)

5.2 Lead Pull Test Data – Lbs

Paste	Ni/Pd/Au Finished Component			Sn/Pb Finished Component		
	min	max	ave	min	max	ave
Sn/Pb	0.80	2.2	1.28	0.60	2.0	1.31
Pb-Free	0.80	2.2	1.31	0.70	2.2	1.29

5.3 Cross Section View of Solder Joint Formation

	Ni/Pd/Au Finished Component	Sn/Pb Finished Component
Sn/Pb Paste		
Pb-Free Paste		

6.0 CYPRESS CONVERSION PLAN

Step 1: Conversion of Tin/Lead lead finish to Nickel/Palladium/Gold finish.

This will be a pre-requisite to enabling full Pb-free solder joint with high reflow temperature. Nickel/Palladium/Gold finish components will be completely compatible and no changes will be done with customer's existing operation environment.

7.0 SUMMARY AND CONCLUSION

Cypress Small Outline (SO) packages (ie. SOIC 20/24L, SSOP48/56L, TSSOP 16/20L) assembled with Nickel/Palladium/Gold finish leadframes passed requirements for component reliability, criteria for solderability test and demonstrated good performance results in actual board mount tests. Other Cypress packages will be converted to Nickel/Palladium/Gold finish per the above conversion plan.

Conversion to Nickel/Palladium/Gold finish requires no changes with customer's existing lines as Solectron board mount data demonstrates in section 5.0, eliminating the need for new part numbers.

The Semiconductor industry (Texas Instruments, SGS Thompson, Philips etc) have been shipping devices with Palladium–based lead finish. To date, there are more than 40 billion devices in field with Palladium– based lead finish. Many technical papers, extensive engineering researches and studies have been published on it.

Cypress is fully confident with its process and is not anticipating any technical roadblocks to the conversion plan.

8.0 REFERENCES

1. IPC/EIA J-STD-002A, Joint Industry Standard, Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires October 1998
2. IPC-A-610C, Surface Mount Assemblies January 2000
3. Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits, Douglas Romm, Bernhard Lange, and Donald Abbott, July 2001 from Texas Instrument.
4. A Nickel-Palladium-Gold Integrated Circuit Lead Finish and Its Potential for Solder-Joint Embrittlement, Donald Abbott, Douglas Romm, Bernhard Lange, December 2001 from Texas Instrument.
5. Solectron Technical Center Analytical Laboratory Report, Tuyen Nguyen, March 2002