Recommended PCB Routing Guidelines for a SkyHigh LPDDR4x Devices

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Associated Part Family:S60Axxxx

AN200008 provides general routing guidelines for PCBs designed with a SkyHigh LPDDR4x devices.

1 Introduction

This application note provides general routing guidelines for PCBs (printed circuit board) designed with a SkyHigh LPDDR4x devices. It does not eliminate the need for customer signal integrity/power delivery simulations and should be used as an initial reference towards PCB design with a SkyHigh LPDDR4x devices. Customers should utilize SkyHigh provided IBIS models for signal timing/crosstalk simulations.

If customers cannot meet or beat the recommendations in this application note, detailed simulations should be performed to determine whether the exceptions would impact bus performance.

This document applies to the following SkyHigh devices:

- S60Axxxx LPDDR4x series

2. Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			NC	VDD2	VSS	DNU	DNU
B	DNU	DQ0	VDDQ	DQ7	VDDQ			VDDQ	DQ15	VDDQ	DQ8	DNU
C	VSS	DQ1	DMI0	DQ6	VSS			VSS	DQ14	DMI1	DQ9	VSS
D	VDDQ	VSS	DQS0_t	VSS	VDDQ			VDDQ	VSS	DQS1_t	VSS	VDDQ
E	VSS	DQ2	DQS0_c	DQ5	VSS			VSS	DQ13	DQS1_c	DQ10	VSS
F	VDD1	DQ3	VDDQ	DQ4	VDD2			VDD2	DQ12	VDDQ	DQ11	VDD1
G	VSS	NC	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0	NC	CS	VDD2			VDD2	CA2	CA3	CA4	VDD2
J	VSS	CA1	VSS	CKE	NC			CLK_t	CLK_c	VSS	CA5	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	NC	VSS	NC	NC			NC	NC	VSS	NC	VSS
R	VDD2	NC	NC	NC	VDD2			VDD2	NC	NC	NC	VDD2
T	VSS	NC	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	NC	VDDQ	NC	VDD2			VDD2	NC	VDDQ	NC	VDD1
V	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
W	VDDQ	VSS	NC	VSS	VDDQ			VDDQ	VSS	NC	VSS	VDDQ
Y	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
AA	DNU	NC	VDDQ	NC	VDDQ			VDDQ	NC	VDDQ	NC	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU
	1	2	3	4	5			8	9	10	11	12

Figure 1- 200 Ball Ball Grid Array

3. Pin Description

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code.
CS	Input	**Chip Select:** CS is part of the command code.
CA[5:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table.
DQ[15:0]	I/O	**Data Input/Output:** Bi-direction data bus.
DQS[1:0]_t, DQS[1:0]_c	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair.
DMI[1:0]	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor.
VDDQ, VDD1, VDD2	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

4. PCB Layers

4.1 PCB Layer Assign Concept Guide

Figure 4.1-1 shows recommended PCB layer assignment. The figure shows the recommended allocation of PCB layers. By using GND as a reference, interference between signal lines can be reduced. And it is easy to secure a design space that can match the length of the signal lines through the dispersion arrangement of the signal lines.

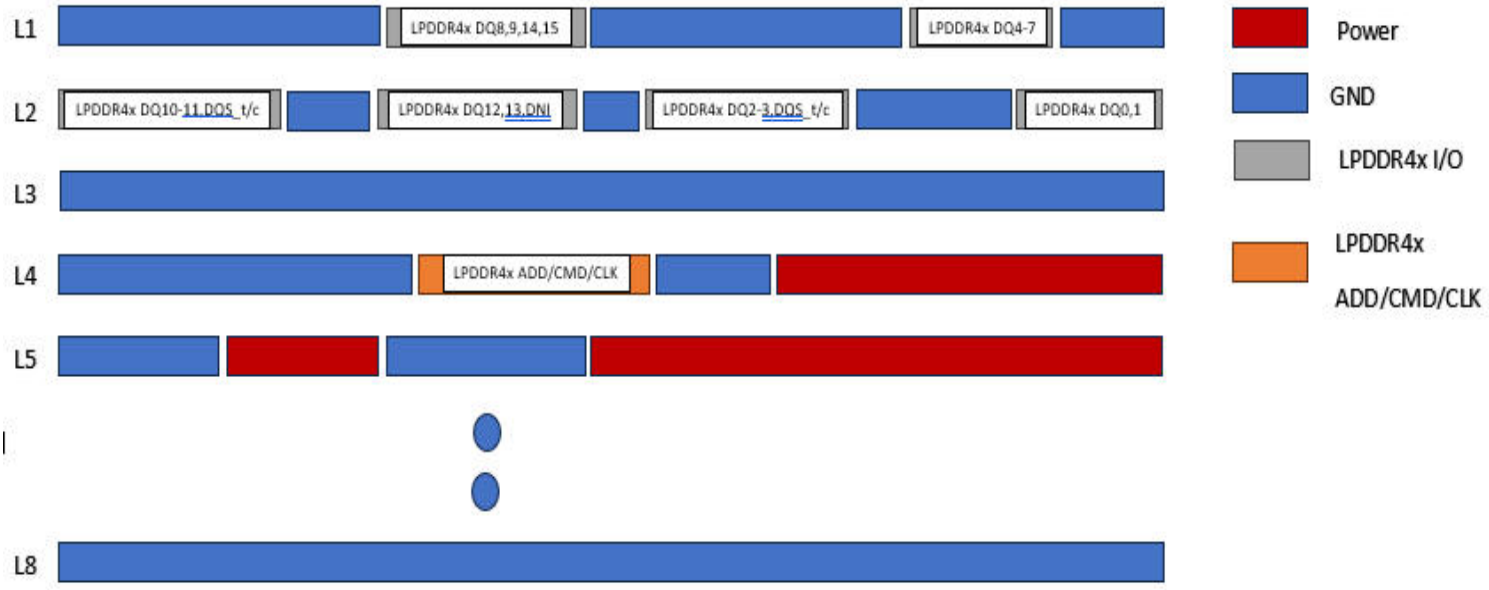

Figure 4.1-1 Recommended PCB Layer Assign(LPDDR4x 1CH)

Pros.	Cons.
Skew reduction between signal lines.	Increase number of layer assign for LPDDR4x.
Crosstalk reduction between signal lines.	-

Notes:

1. In LPDDR4x package of SkyHigh, DQ length is managed within+/-1mm based on DQS. CA length is managed within +/-2mm based on CLK. Differential pair (DQS/CLK) is managed within 0.1mm between differential pairs.
2. If per pin training is applied and working properly, signal net skew will be compensated.

4.2 PCB Layer Assign Concept Guide(Cont'd)

Figure 4.2-1 shows another recommended PCB layer assignment. The number of PCB layers assigned to LPDDR4x products can be reduced. However, it is difficult to match the length between the signal lines, so the skew between the signal lines can be increased. The layer assignments below should follow the 2*W[2] or 3*H[3] design rules to reduce signal crosstalk.

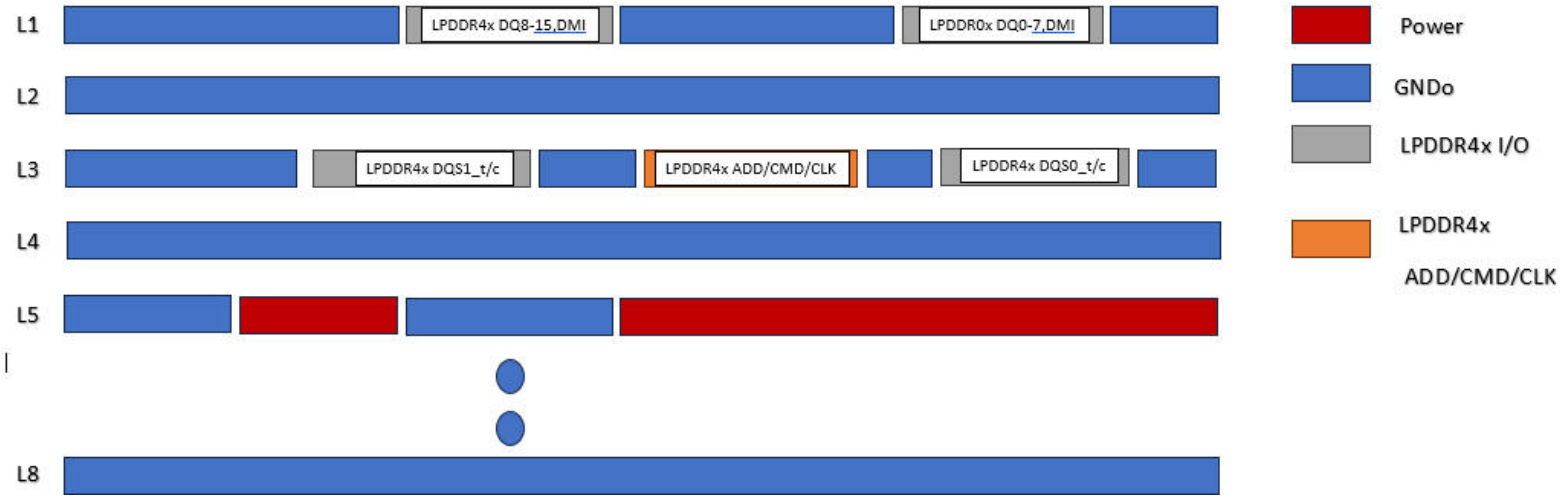

Figure 4.2-1 Another Recommended PCB Layer Assign(LPDDR4x 1CH)

Pros.	Cons.
Minimize the number of layer assign for LPDDR4x	Increase skew between signal lines.
-	Increase Crosstalk between signal lines.

Notes:

1. In LPDDR4x package of SkyHigh, DQ length is managed within +/- 1mm based on DQS. CA length is managed within +/- 2mm based on CLK. Differential pair(DQS/CLK) is managed within 0.1mm between differential pairs.
2. W is the width of signal trace.
3. H is the height of dielectric material between signal and reference(GND) layer.
4. If per pin training is applied and working properly, signal net skew will be compensated.

5. PCB Design Guide

5.1 Signal Design Guide

5.1.1 LPDDR4x SDRAM

The Table 4.1.1 shows the recommended design guide for the system board. The Guide is for the SkyHigh LPDDR4x SDRAM. And there are things that are related to each other. In particular, the length and impedance are influenced by the cross talk

Item	Guide Value			Remark
LPDDR4x Speed	I/O 3200Mbps CA 1600Mbps	I/O 3733Mbps CA 1866Mbps	I/O 4266Mbps CA 2133Mbps	2 Loading (2 Dies/Pin)
I/O Signal Length (DQ, DQS_t/c)	≤ 20mm	≤ 15mm	≤ 12mm	
ADD/CMD Signal Length (CA, CLK_t/c)	≤ 25mm	≤ 20mm	≤ 20mm	3 Loading (3 Dies/Pin)
Single-ended Signal Z_0	45ohms +/- 5%			[1] Term.(ODT) & No-Term.
Differential Signal Zdiff	90ohms +/- 5%			
Space between Single-ended Signal line	The bigger of ≥ 2W[2], ≥ 3H[3]			Crosstalk
Space between Differential Pair line and Other Signal line	The bigger of (≥ 2W, ≥ 2S[4]) or GND Shield			
Delta Trace Length of Single-ended Signal	≤ 2mm (It does not matter if the per pin training function is applied.)			Skew
Delta Trace Length of Differential Pair Signal	≤ 0.5mm			

Table 4.1.1 Recommended Guide for LPDDR4x

Notes:

1. Considers both the termination and no_term operating condition.
2. W is the width of signal trace.
3. H is the height of dielectric material between signal and reference(GND) layer.
4. S means the space between differential signal traces.
5. It can be changed according to the operation condition(SoC type, Drive Strength, ODT(Term.) resister and so on...) of system.

5. PCB Design Guide

5.2 PDN Design Guide

5.2.1 LPDDR4x SDRAM

The PDN(Power Delivery Network) is a very important factor for all devices to operate reliably. Therefore, great care should be given in designing the PDN to ensure a stable and uniform voltage supply. The DRAM package has 2 channels (CH. A, CH. B), where decoupling capacitors should be mounted as close to the DRAM ball group of each channel as possible in order to meet the PDN impedance requirements. The Table 4.2.1 shows the PDN guide for all power types of LPDDR4x. And ESR and ESL of De-cap. are very important for board capacitors as seen in Figure 3.1. It is recommended that you choose the appropriate ESR and ESL value for the decoupling capacitor size.

Power	Channel	Target DC R	Target AC Z @20MHz
VDD1 (1.8V)	CH. A	< 103mΩ	< 153mΩ
	CH. B	< 103mΩ	< 153mΩ
VDD2 (1.1V)	CH. A	< 17mΩ	< 21mΩ
	CH. B	< 17mΩ	< 21mΩ
VDDQ (0.6V)	CH. A	< 22mΩ	< 45mΩ
	CH. B	< 22mΩ	< 45mΩ

Table 4.2.1 PDN Guide for LPDDR4x (max. 4 Die Stack/Channel)

Notes:

1. The DC R & AC Z target is limited to LPDDR4x products
2. Target impedance is defined for all pins per voltage domain per channel. Target impedance does not include the DRAM package and silicon die.

6. Document History Page

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